

# Preliminary

Notice: This is not a final specification.  
Some parametric limits are subject to change.

Renesas LSIs

## M5M29KB/T641ATP

67,108,864-BIT (8,388,608-WORD BY 8-BIT /4,194,304-WORD BY 16-BIT)  
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

### DESCRIPTION

The M5M29KB/T641ATP are 3.3V-only high speed 67,108,864-bit CMOS boot block FLASH Memories with alternating BGO(Back Ground Operation) feature. The BGO feature of the device allows Program or Erase operations to be performed in one bank while the device simultaneously allows Read operations to be performed on the other bank.

This BGO feature is suitable for mobile and personal computing, and communication products.

The M5M29KB/T641ATP are fabricated by CMOS technology for the peripheral circuit and DINOR IV(Divided bit-line NOR IV) architecture for the memory cell, and are available in 52pin TSOP(II) for lead free use.

M5M29KB/T641ATP provides for Software Lock Release function. Usually, all memory blocks are locked and can not be programmed or erased, when WP# is low. Using Software Lock Release function, program or erase operation can be executed.

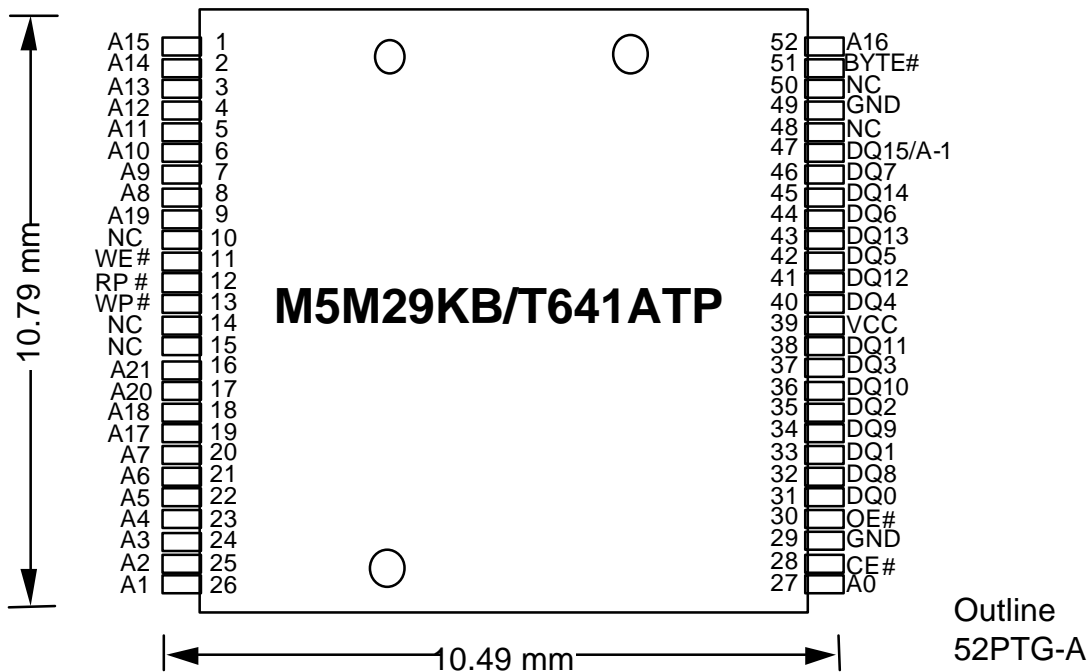
### FEATURES

Access time	Random	70ns (Max.)
	Page	25ns(Max.)
Supply voltage		VCC= 3.0 ~ 3.6V
Ambient temperature		Ta=-40 ~ 85 °C
Package	52pin TSOP(Type-II), Lead pitch 0.4mm	
	Outer-lead finishing : Sn-Cu	

### APPLICATION

Digital Cellar Phone, Telecommunication,  
PDA, Car Navigation System, Video Game Machine

PIN CONFIGURATION (TOP VIEW)



VCC : VCC  
GND : GND  
A0-A21 : Address  
DQ0-DQ15 : Data I/O  
CE# : Chip enable  
OE# : Output enable

WE# : Write enable  
WP# : Write protect  
RP# : Reset power down  
BYTE# : Byte enable

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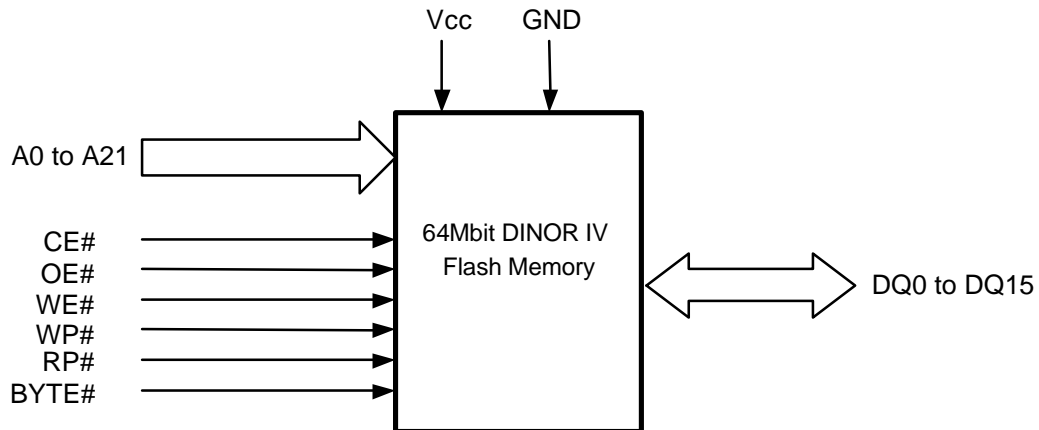
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CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

### 64M Flash Memory Block Diagram



### Capacitance

Symbol	Parameter		Conditions	Limits			Unit
				Min.	Typ.	Max.	
CIN	Input capacitance	A21-A0, OE#, WE#, CE#, WP#, RP#, BYTE#	Ta=25°C, f=1MHz, Vin=Vout=0V			12	pF
COUT	Output Capacitance	DQ15-DQ0				12	pF

### Flash Memory Part

#### Description

The 64M-bit DINOR IV(Divided bit line NOR IV) Flash Memory is 3.3V-only high speed 67,108,864-bit CMOS boot block Flash Memory. Alternating BGO(Back Ground Operation) feature of the device allows Program or Erase operations to be performed in one bank while the device simultaneously allows Read operations to be performed on the other bank. This BGO feature is suitable for communication products and cellular phone. The Flash Memory is fabricated by CMOS technology for the peripheral circuits and DINOR IV architecture for the memory cells.

- Auto Erase
 

Erase time	Main Block	150ms/block (typ.)
------------	------------	--------------------
- Erase unit
 

Bank(I)	Boot Block	4K-word x2/ 8K-byte x2
	Parameter Block	4K-word x6 / 8K-byte x6
	Main Block	32K-word x7 / 64K-byte x7
Bank(II)	Main Block	32K-word x8 / 64K-byte x8
Bank(III)	Main Block	32K-word x24 / 64K-byte x56
Bank(IV)	Main Block	32K-word x24 / 64K-byte x56
- Program/Erase cycles 100Kcycles
- Boot Block
 

Bottom Boot	M***B6*****
Top Boot	M***T6*****
- The Other Functions
  - Software Command Control
  - Software Lock Release(while WP# is low)
  - Erase Suspend/Resume
  - Program Suspend/Resume
  - Status Register Read
  - Alternating Back Ground Program/Erase Operation Between Bank(I), Bank(II), Bank(III) and Bank(IV)
  - Random Page Read

#### Features

- Organization 4,194,304-word x 16-bit  
8,388,608-byte x 8-bit
- Supply Voltage VCC = 3.0 ~ 3.6V
- Access time
 

Random Access	70ns(Max.)
Random Page Read	25ns(Max.)
- Read 108mW (Max. at 5MHz)  
(After Automatic Power Down) 0.33μW(typ.)
- Program/Erase 126mW(Max.)
- Standby 0.33μW(typ.)
- Deep Power Down mode 0.33μW(typ.)
- Auto Program for Bank(I) – Bank(IV)
 

Program Time	
Word Program	30μs/word(typ.)
Byte Program	30μs/byte(typ.)
Page Program	4ms(typ.)
Program Unit	
Word/Byte Program	1word/ 1byte
Page Program	128 words/ 256 bytes

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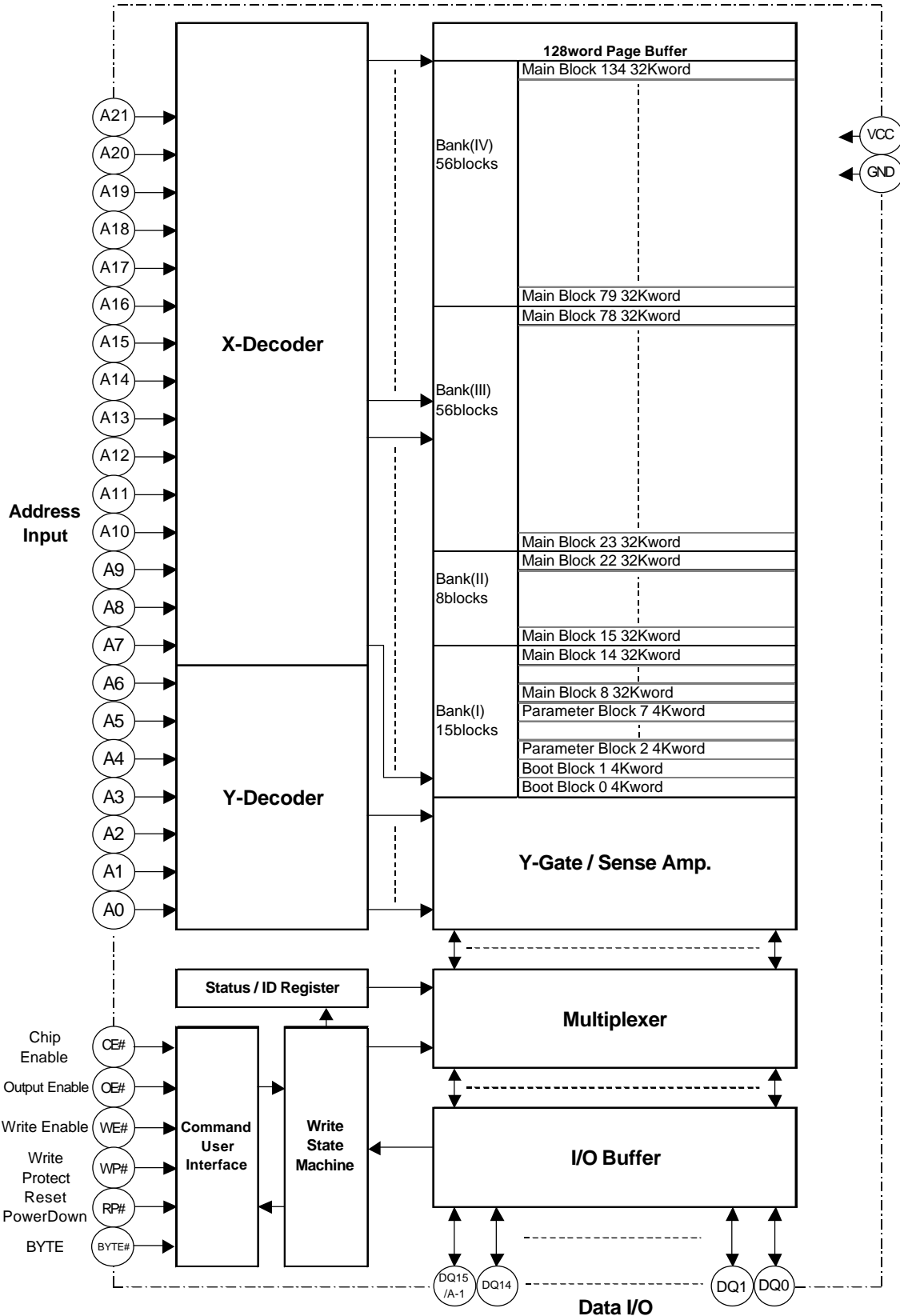
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CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

Block Diagram (64Mbit Flash Memory)



### Function of Flash Memory

The 64M-bit DINOR IV Flash Memory includes on-chip program/erase control circuitry. The Write State Machine (WSM) controls block erase and word/page program operations. Operational modes are selected by the commands written to the Command User Interface (CUI). The Status Register indicates the status of the WSM and when the WSM successfully completes the desired program or block erase operation.

A Deep Power Down mode is enabled when the RP# pin is at GND, minimizing power consumption.

### Read

The 64M-bit DINOR IV Flash Memory has four read modes, which accesses to the memory array, the Page read, the Device Identifier and the Status Register. The appropriate read commands are required to be written to the CUI. Upon initial device power up or after exit from deep power down, the 64M-bit DINOR IV Flash Memory automatically resets to read array mode. In the read array mode and in the conditions are low level input to OE#, high level input to WE# and RP#, low level input to CE# and address signals to the address inputs (A21 - A0: Word mode / A21-A-1: Byte mode) the data of the addressed location to the data input/output (DQ15-DQ0: Word mode / DQ7- DQ0: Byte mode) is output.

### Write

Writes to the CUI enables reading of memory array data, device identifiers and reading and clearing of the Status Register. They also enable block erase and program. The CUI is written by bringing WE# to low level and OE# is at high level, while CE# is at low level. Address and data are latched on the earlier rising edge of WE# and CE#. Standard micro processor write timings are used.

### Alternating Background Operation (BGO)

The 64M-bit DINOR IV Flash Memory allows to read array from one bank while the other bank operates in software command write cycling or the erasing / programming operation in the background. Array Read operation with the other bank in BGO is performed by changing the bank address without any additional command. When the bank address points the bank in software command write cycling or the erasing / programming operation, the data is read out from the status register. The access time with BGO is the same as the normal read operation. BGO must be between Bank(I), Bank(II), Bank(III) and Bank(IV).

### Output Disable

When OE# is at VIH, output from the devices is disabled. Data input/output are in a high-impedance (High-Z) state.

### Standby

When CE# is at VIH, the device is in the standby mode and its power consumption is reduced. Data input/output are in a high-impedance (High-Z) state. If the memory is deselected during block erase or program, the internal control circuits remain active and the device consumes normal active power until the operation completes.

### Deep Power Down

When RP# is at VIL, the device is in the deep power down mode and its power consumption is substantially low. During read modes, the memory is deselected and the data input/output are in a high-impedance (High-Z) state. After return from power down, the CUI is reset to Read Array, and the Status Register is cleared to value 80H.

During block erase or program modes, RP# low will abort either operation. Memory array data of the block being altered become invalid.

### Automatic Power Down (Auto-PD)

The Automatic Power Down minimizes the power consumption during read mode. The device automatically turns to this mode when any addresses or CE# isn't changed more than 200ns after the last alternation. The power consumption becomes the same as the stand-by mode. During this mode, the output data is latched and can be read out. New data is read out correctly when addresses are changed.

### BBR(Back Bank array Read)

In the 64M-bit DINOR IV Flash Memory, when one memory address is read according to a Read Mode in the case of the same as an access when a Read Mode command is input, another Bank memory data can be read out (Random) by changing another Bank address.

### Software Command Definitions

The device operations are selected by writing specific software command into the Command User Interface.

#### Read Array Command (FFH)

The device is in Read Array mode on initial device power up and after exit from deep power down, or by writing FFH to the Command User Interface. After starting the internal operation the device is set to the read status register mode automatically.

#### Read Device Identifier Command (90H)

We can normally read device identifier codes when Read Device Identifier Code Command (90H) is written to the command latch. Following the command write, the manufacturer code and the device code can be read from A0 address 0H and 1H in a bank address, respectively.

#### Read Status Register Command (70H)

The Status Register is read after writing the Read Status Register command of 70H to the Command User Interface. Also, after starting the internal operation the device is set to the Read Status Register mode automatically.

The contents of Status Register are latched on the later falling edge of OE# or CE#. When status read is required, OE# or CE# must be toggled every status read.

#### Page Read Command (F3H)

The Page Read command (F3H) timing can be used by writing the first command to CUI and CE# falls VIL or changing the address(A21-A2) is necessary to start activating page read mode. This command is fast random 4 words read. During the read it is necessary to fix CE# low and change addresses that are defined by A0 and A1(0h - 3h) at random continuously. The mode is kept until RP# is set to L or this chip is powered down.

The first read of Page Read timing is the same as normal read (ta(CE)). CE# should be fallen "L". The read timing after the first is the same as ta(PAD).

In the page read mode the upper address(A21-A2) or CE# are supposed not to be clocked during read operation. Otherwise the access time is as same as normal read.

### Clear Status Register Command (50H)

The Erase Status, Program Status and Block Status bits are set to "1"s by the Write State Machine and can only be reset by the Clear Status Register command of 50H. These bits indicate various failure conditions.

### Block Erase / Confirm Command (20H/D0H)

Automated block erase is initiated by writing the Block Erase command of 20H followed by the Confirm command of D0H. An address within the block to be erased is required. The WSM executes iterative erase pulse application and erase verify operation.

### Program Commands

#### A) Word / Byte Program (40H)

Word / Byte program is executed by a two-command sequence. The Word/Byte program Setup command of 40H is written to the Command Interface, followed by a second write specifying the address and data to be written. The WSM controls the program pulse application and verify operation.

#### B) Page Program for Data Blocks (41H)

Page Program allows fast programming of 128 words/ 256 bytes of data. Writing of 41H initiates the page program operation for the Data area. From 2nd cycle to 129th cycle(Word mode)/ 257th cycle(Byte mode), write data must be serially inputted. Address A6-A0(Word mode)/ A6-A-1(Byte mode) have to be incremented from 00H to 7FH. After completion of data loading, the WSM controls the program pulse application and verify operation.

#### C) Single Data Load to Page Buffer (74H)

##### / Page Buffer to Flash (0EH/D0H)

Single data load to the page buffer is performed by writing 74H followed by a second write specifying the column address and data. Distinct data up to 128word can be loaded to the page buffer by this two-command sequence. On the other hand, all of the loaded data to the page buffer is programmed simultaneously by writing Page Buffer to Flash command of 0EH followed by the confirm command of D0H. After completion of programming the data on the page buffer is cleared automatically.

### Flash to Page Buffer Command (F1H/D0H)

Array data load to the page buffer is performed by writing the Flash to Page Buffer command of F1H followed by the Confirm command of D0H. An address within the page to be loaded is required. Then the array data can be copied into the other pages within the same bank by using the Page Buffer to Flash command.

### Clear Page Buffer Command (55H/D0H)

Loaded data to the page buffer is cleared by writing the Clear Page Buffer command of 55H followed by the Confirm command of D0H. This command is valid for clearing data loaded by Single Data Load to Page Buffer command.

### Data Protection

The 64M-bit DINOR IV Flash Memory has a master Write Protect pin (WP#). When WP# is at VIH, all blocks can be programmed or erased. When WP# is low, all blocks are in locked mode which prevents any modifications to memory blocks. Software Lock Release function is only command which allows to program or erase.

### Suspend/Resume Command (B0H/D0H)

Writing the Suspend command of B0H during block erase operation interrupts the block erase operation and allows read out from another block of memory. Writing the Suspend command of B0H during program operation interrupts the program operation and allows read out from another block of memory. The Bank address is required when writing the Suspend/Resume Command. The device continues to output Status Register data when read, after the Suspend command is written to it. Polling the WSM Status and Suspend Status bits will determine when the erase operation or program operation has been suspended. At this point, writing of the Read Array command to the CUI enables reading data from blocks other than that which is suspended. When the Resume command of D0H is written to the CUI, the WSM will continue with the erase or program processes.

### Erase All Unlocked Blocks Command (A7H/D0H)

The command sequence enable us to erase all blocks. The command can be used by writing Setup command A7H(1<sup>st</sup> cycle) and confirm command D0H(2<sup>nd</sup> cycle). The sequence is not valid in case of WP#=VIL.

### Power Supply Voltage

When the power supply voltage is less than VLKO, Low VCC Lock-Out voltage, the device is set to the Read-only mode.

A delay time of 60 $\mu$ s is required before any device operation is initiated. The delay time is measured from the time Flash VCC reaches Flash VCCmin (3.0V).

During power up, RP# = GND is recommended. Falling in Busy status is not recommended for possibility of damaging the device.

### Memory Organization

The 64M-bit DINOR IV Flash Memory is constructed by 2 boot blocks of 4K words/ 8K bytes, 6 parameter blocks of 4K words/ 8K bytes and 7 main blocks of 32K words/ 64K bytes in Bank(I), by 8 main blocks of 32K words/ 64K bytes in Bank(II) and by 56 main blocks of 32K words/ 64K bytes in Bank(III) and Bank(IV).

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CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

## Block Organization

## 64M-bit DINOR(IV) Flash Memory Map (Bottom Boot)

x8 (Byte Mode) x16 (Word Mode)

1A0000H-1AFFFFH	D0000H-D7FFFFH	32Kword 33
190000H-19FFFFH	C8000H-CFFFFH	32Kword 32
180000H-18FFFFH	C0000H-C7FFFFH	32Kword 31
170000H-17FFFFH	B8000H-BFFFFH	32Kword 30
160000H-16FFFFH	B0000H-B7FFFFH	32Kword 29
150000H-15FFFFH	A8000H-AFFFFH	32Kword 28
140000H-14FFFFH	A0000H-A7FFFFH	32Kword 27
130000H-13FFFFH	98000H-9FFFFH	32Kword 26
120000H-12FFFFH	90000H-97FFFFH	32Kword 25
110000H-11FFFFH	88000H-8FFFFH	32Kword 24
100000H-10FFFFH	80000H-7FFFFH	32Kword 23
F0000H-FFFFFH	78000H-7FFFFH	32Kword 22
E0000H-EFFFFH	70000H-77FFFFH	32Kword 21
D0000H-DFFFFH	68000H-6FFFFH	32Kword 20
C0000H-CFFFFH	60000H-67FFFFH	32Kword 19
B0000H-BFFFFH	58000H-5FFFFH	32Kword 18
A0000H-AFFFFH	50000H-57FFFFH	32Kword 17
90000H-9FFFFH	48000H-4FFFFH	32Kword 16
80000H-8FFFFH	40000H-47FFFFH	32Kword 15
70000H-7FFFFH	38000H-3FFFFH	32Kword 14
60000H-6FFFFH	30000H-37FFFFH	32Kword 13
50000H-5FFFFH	28000H-27FFFFH	32Kword 12
40000H-4FFFFH	20000H-27FFFFH	32Kword 11
30000H-3FFFFH	18000H-1FFFFH	32Kword 10
20000H-2FFFFH	10000H-17FFFFH	32Kword 9
10000H-1FFFFH	08000H-0FFFFH	32Kword 8
0E000H-0FFFFH	07000H-07FFFFH	4Kword 7
0C000H-0DFFFFH	06000H-06FFFFH	4Kword 6
0A000H-0BFFFFH	05000H-05FFFFH	4Kword 5
08000H-09FFFFH	04000H-04FFFFH	4Kword 4
06000H-07FFFFH	03000H-03FFFFH	4Kword 3
04000H-05FFFFH	02000H-02FFFFH	4Kword 2
02000H-03FFFFH	01000H-01FFFFH	4Kword 1
00000H-01FFFFH	00000H-00FFFFH	4Kword 0

BANK(III)

BANK(II)

BANK(I)

x8 (Byte Mode) x16 (Word Mode)

3C0000H-3CFFFFH	1E0000H-1E7FFFFH	32Kword 67
3B0000H-3BFFFFH	1D8000H-1DFFFFH	32Kword 66
3A0000H-3AFFFFH	1D0000H-1D7FFFFH	32Kword 65
390000H-39FFFFH	1C8000H-1CFFFFH	32Kword 64
380000H-38FFFFH	1C0000H-1C7FFFFH	32Kword 63
370000H-37FFFFH	1B8000H-1BFFFFH	32Kword 62
360000H-36FFFFH	1B0000H-1B7FFFFH	32Kword 61
350000H-35FFFFH	1A8000H-1AFFFFH	32Kword 60
340000H-34FFFFH	1A0000H-1A7FFFFH	32Kword 59
330000H-33FFFFH	198000H-19FFFFH	32Kword 58
320000H-32FFFFH	190000H-197FFFFH	32Kword 57
310000H-31FFFFH	188000H-18FFFFH	32Kword 56
300000H-30FFFFH	180000H-187FFFFH	32Kword 55
2F0000H-2FFFFFH	178000H-17FFFFH	32Kword 54
2E0000H-2EFFFFH	170000H-177FFFFH	32Kword 53
2D0000H-2DFFFFH	168000H-16FFFFH	32Kword 52
2C0000H-2CFFFFH	160000H-167FFFFH	32Kword 51
2B0000H-2BFFFFH	158000H-15FFFFH	32Kword 50
2A0000H-2AFFFFH	150000H-157FFFFH	32Kword 49
290000H-29FFFFH	148000H-14FFFFH	32Kword 48
280000H-28FFFFH	140000H-147FFFFH	32Kword 47
270000H-27FFFFH	138000H-137FFFFH	32Kword 46
260000H-26FFFFH	130000H-137FFFFH	32Kword 45
250000H-25FFFFH	128000H-12FFFFH	32Kword 44
240000H-24FFFFH	120000H-127FFFFH	32Kword 43
230000H-23FFFFH	118000H-11FFFFH	32Kword 42
220000H-22FFFFH	110000H-117FFFFH	32Kword 41
210000H-21FFFFH	108000H-10FFFFH	32Kword 40
200000H-20FFFFH	100000H-107FFFFH	32Kword 39
1F0000H-1FFFFFH	F8000H-F7FFFFH	32Kword 38
1E0000H-1EFFFFH	F0000H-F7FFFFH	32Kword 37
1D0000H-1DFFFFH	E8000H-E7FFFFH	32Kword 36
1C0000H-1CFFFFH	E0000H-E7FFFFH	32Kword 35
1B0000H-1BFFFFH	D8000H-D7FFFFH	32Kword 34

BANK(III)

x8 (Byte Mode) x16 (Word Mode)

5E0000H-5EFFFFH	2F0000H-2F7FFFFH	32Kword 101
5D0000H-5DFFFFH	2E8000H-2EFFFFH	32Kword 100
5C0000H-5CFFFFH	2E0000H-2E7FFFFH	32Kword 99
5B0000H-5BFFFFH	2D8000H-2DFFFFH	32Kword 98
5A0000H-5AFFFFH	2D0000H-2D7FFFFH	32Kword 97
590000H-59FFFFH	2C8000H-2CFFFFH	32Kword 96
580000H-58FFFFH	2C0000H-2C7FFFFH	32Kword 95
570000H-57FFFFH	2B8000H-2BFFFFH	32Kword 94
560000H-56FFFFH	2B0000H-2B7FFFFH	32Kword 93
550000H-55FFFFH	2A8000H-2AFFFFH	32Kword 92
540000H-54FFFFH	2A0000H-2A7FFFFH	32Kword 91
530000H-53FFFFH	298000H-29FFFFH	32Kword 90
520000H-52FFFFH	290000H-297FFFFH	32Kword 89
510000H-51FFFFH	288000H-28FFFFH	32Kword 88
500000H-50FFFFH	280000H-287FFFFH	32Kword 87
4F0000H-4FFFFH	278000H-27FFFFH	32Kword 86
4E0000H-4EFFFFH	270000H-277FFFFH	32Kword 85
4D0000H-4DFFFFH	268000H-26FFFFH	32Kword 84
4C0000H-4CFFFFH	260000H-267FFFFH	32Kword 83
4B0000H-4BFFFFH	258000H-25FFFFH	32Kword 82
4A0000H-4AFFFFH	250000H-257FFFFH	32Kword 81
490000H-49FFFFH	248000H-247FFFFH	32Kword 80
480000H-48FFFFH	240000H-247FFFFH	32Kword 79
470000H-47FFFFH	238000H-23FFFFH	32Kword 78
460000H-46FFFFH	230000H-237FFFFH	32Kword 77
450000H-45FFFFH	228000H-22FFFFH	32Kword 76
440000H-44FFFFH	220000H-227FFFFH	32Kword 75
430000H-43FFFFH	218000H-21FFFFH	32Kword 74
420000H-42FFFFH	210000H-217FFFFH	32Kword 73
410000H-41FFFFH	208000H-207FFFFH	32Kword 72
400000H-40FFFFH	200000H-207FFFFH	32Kword 71
3F0000H-3FFFFH	1F8000H-1FFFFFH	32Kword 70
3E0000H-3EFFFFH	1F0000H-1F7FFFFH	32Kword 69
3D0000H-3DFFFFH	1E8000H-1E7FFFFH	32Kword 68

BANK(IV)

BANK(III)

x8 (Byte Mode) x16 (Word Mode)

7F0000H-7FFFFFH	3F8000H-3FFFFFH	32Kword 134
7E0000H-7EFFFFH	3F0000H-3F7FFFFH	32Kword 133
7D0000H-7DFFFFH	3E8000H-3EFFFFH	32Kword 132
7C0000H-7CFFFFH	3E0000H-3E7FFFFH	32Kword 131
7B0000H-7BFFFFH	3D8000H-3DFFFFH	32Kword 130
7A0000H-7AFFFFH	3D0000H-3D7FFFFH	32Kword 129
790000H-79FFFFH	3C8000H-3CFFFFH	32Kword 128
780000H-78FFFFH	3C0000H-3C7FFFFH	32Kword 127
770000H-77FFFFH	3B8000H-3BFFFFH	32Kword 126
760000H-76FFFFH	3B0000H-3B7FFFFH	32Kword 125
750000H-75FFFFH	3A8000H-3AFFFFH	32Kword 124
740000H-74FFFFH	3A0000H-3A7FFFFH	32Kword 123
730000H-73FFFFH	398000H-39FFFFH	32Kword 122
720000H-72FFFFH	390000H-397FFFFH	32Kword 121
710000H-71FFFFH	388000H-387FFFFH	32Kword 120
700000H-70FFFFH	380000H-387FFFFH	32Kword 119
6F0000H-6FFFFH	378000H-377FFFFH	32Kword 118
6E0000H-6EFFFFH	370000H-377FFFFH	32Kword 117
6D0000H-6DFFFFH	368000H-367FFFFH	32Kword 116
6C0000H-6CFFFFH	360000H-367FFFFH	32Kword 115
6B0000H-6BFFFFH	358000H-357FFFFH	32Kword 114
6A0000H-6AFFFFH	350000H-357FFFFH	32Kword 113
690000H-69FFFFH	348000H-347FFFFH	32Kword 112
680000H-68FFFFH	340000H-347FFFFH	32Kword 111
670000H-67FFFFH	338000H-337FFFFH	32Kword 110
660000H-66FFFFH	330000H-337FFFFH	32Kword 109
650000H-65FFFFH	328000H-327FFFFH	32Kword 108
640000H-64FFFFH	320000H-327FFFFH	32Kword 107
630000H-63FFFFH	318000H-317FFFFH	32Kword 106
620000H-62FFFFH	310000H-317FFFFH	32Kword 105
610000H-61FFFFH	308000H-307FFFFH	32Kword 104
600000H-60FFFFH	300000H-307FFFFH	32Kword 103
5F0000H-5FFFFH	2F8000H-2F7FFFFH	32Kword 102

BANK(IV)



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CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

## Block Organization

## 64M-bit DINOR(IV) Flash Memory Map (Top Boot)

x8 (Byte Mode)	x16 (Word Mode)	x8 (Byte Mode)	x16 (Word Mode)	x8 (Byte Mode)	x16 (Word Mode)	x8 (Byte Mode)	x16 (Word Mode)
210000H-21FFFFH	108000H-10FFFFH	430000H-43FFFFH	218000H-21FFFFH	650000H-65FFFFH	328000H-32FFFFH	7FE000H-7FFFFFH	3FF000H-3FFFFFH
200000H-20FFFFH	100000H-10FFFFH	420000H-42FFFFH	210000H-21FFFFH	640000H-64FFFFH	320000H-32FFFFH	7FC000H-7FDFFFH	3FE000H-3FEFFFH
1F0000H-1FFFFFH	F8000H-FFFFFH	410000H-41FFFFH	208000H-20FFFFH	630000H-63FFFFH	318000H-31FFFFH	7FA000H-7FBFFFH	3FD000H-3FDFFFH
1E0000H-1EFFFFH	F0000H-F7FFFH	400000H-40FFFFH	200000H-20FFFFH	620000H-62FFFFH	310000H-317FFFH	7F8000H-7F9FFFH	3FC000H-3FCFFFH
1D0000H-1DFFFFH	E8000H-E7FFFH	3F0000H-3FFFFFH	1F8000H-1F7FFFH	610000H-61FFFFH	308000H-30FFFFH	7F6000H-7F7FFFH	3FB000H-3FBFFFH
1C0000H-1CFFFFH	E0000H-E7FFFH	3E0000H-3EFFFFH	1F0000H-1F7FFFH	600000H-60FFFFH	300000H-307FFFH	7F4000H-7F5FFFH	3FA000H-3FAFFFH
1B0000H-1BFFFFH	D8000H-D7FFFH	3D0000H-3DFFFFH	1E8000H-1E7FFFH	5F0000H-5FFFFFH	2F8000H-2F7FFFH	7F2000H-7F3FFFH	3F9000H-3F9FFFH
1A0000H-1AFFFFH	D0000H-D7FFFH	3C0000H-3CFFFFH	1E0000H-1E7FFFH	5E0000H-5EFFFFH	2F0000H-2F7FFFH	7F0000H-7F1FFFH	3F8000H-3F8FFFH
190000H-19FFFFH	C8000H-C7FFFH	3B0000H-3BFFFFH	1D8000H-1D7FFFH	5D0000H-5DFFFFH	2E8000H-2E7FFFH	7E0000H-7E1FFFH	3F7000H-3F7FFFH
180000H-18FFFFH	C0000H-C7FFFH	3A0000H-3AFFFFH	1D0000H-1D7FFFH	5C0000H-5CFFFFH	2E0000H-2E7FFFH	7D0000H-7D1FFFH	3E8000H-3E8FFFH
170000H-17FFFFH	B8000H-B7FFFH	390000H-39FFFFH	1C8000H-1C7FFFH	5B0000H-5BFFFFH	2D8000H-2D7FFFH	7C0000H-7C1FFFH	3E7000H-3E7FFFH
160000H-16FFFFH	B0000H-B7FFFH	380000H-38FFFFH	1C0000H-1C7FFFH	5A0000H-5AFFFFH	2D0000H-2D7FFFH	7B0000H-7B1FFFH	3E6000H-3E6FFFH
150000H-15FFFFH	A8000H-A7FFFH	370000H-37FFFFH	1B8000H-1B7FFFH	590000H-59FFFFH	2C8000H-2C7FFFH	7A0000H-7A1FFFH	3E5000H-3E5FFFH
140000H-14FFFFH	A0000H-A7FFFH	360000H-36FFFFH	1B0000H-1B7FFFH	580000H-58FFFFH	2C0000H-2C7FFFH	790000H-791FFFH	3E4000H-3E4FFFH
130000H-13FFFFH	98000H-97FFFH	350000H-35FFFFH	1A8000H-1A7FFFH	570000H-57FFFFH	2B8000H-2B7FFFH	780000H-781FFFH	3E3000H-3E3FFFH
120000H-12FFFFH	90000H-97FFFH	340000H-34FFFFH	1A0000H-1A7FFFH	560000H-56FFFFH	2B0000H-2B7FFFH	770000H-771FFFH	3E2000H-3E2FFFH
110000H-11FFFFH	88000H-87FFFH	330000H-33FFFFH	198000H-197FFFH	550000H-55FFFFH	2A8000H-2A7FFFH	760000H-761FFFH	3E1000H-3E1FFFH
100000H-10FFFFH	80000H-87FFFH	320000H-32FFFFH	190000H-197FFFH	540000H-54FFFFH	2A0000H-2A7FFFH	750000H-751FFFH	3E0000H-3E0FFFH
F0000H-FFFFFH	78000H-77FFFH	310000H-31FFFFH	188000H-187FFFH	530000H-53FFFFH	298000H-297FFFH	740000H-741FFFH	3D0000H-3D0FFFH
E0000H-EFFFFH	70000H-77FFFH	300000H-30FFFFH	180000H-187FFFH	520000H-52FFFFH	290000H-297FFFH	730000H-731FFFH	3C0000H-3C0FFFH
D0000H-DFFFFH	68000H-67FFFH	2F0000H-2FFFFFH	178000H-177FFFH	510000H-51FFFFH	288000H-287FFFH	720000H-721FFFH	3B0000H-3B0FFFH
C0000H-CFFFFH	60000H-67FFFH	2E0000H-2EFFFFH	170000H-177FFFH	500000H-50FFFFH	280000H-287FFFH	710000H-711FFFH	3B8000H-3B8FFFH
B0000H-BFFFFH	58000H-57FFFH	2D0000H-2DFFFFH	168000H-167FFFH	4F0000H-4FFFFFH	278000H-277FFFH	700000H-701FFFH	3B7000H-3B7FFFH
A0000H-AFFFFH	50000H-57FFFH	2C0000H-2CFFFFH	160000H-167FFFH	4E0000H-4EFFFFH	270000H-277FFFH	6F0000H-6F1FFFH	3B6000H-3B6FFFH
90000H-9FFFFH	48000H-47FFFH	2B0000H-2BFFFFH	158000H-157FFFH	4D0000H-4DFFFFH	268000H-267FFFH	6E0000H-6E1FFFH	3B5000H-3B5FFFH
80000H-8FFFFH	40000H-47FFFH	2A0000H-2AFFFFH	150000H-157FFFH	4C0000H-4CFFFFH	260000H-267FFFH	6D0000H-6D1FFFH	3B4000H-3B4FFFH
70000H-7FFFFH	38000H-37FFFH	290000H-29FFFFH	148000H-147FFFH	4B0000H-4BFFFFH	258000H-257FFFH	6C0000H-6C1FFFH	3B3000H-3B3FFFH
60000H-6FFFFH	30000H-37FFFH	280000H-28FFFFH	140000H-147FFFH	4A0000H-4AFFFFH	250000H-257FFFH	6B0000H-6B1FFFH	3B2000H-3B2FFFH
50000H-5FFFFH	28000H-27FFFH	270000H-27FFFFH	138000H-137FFFH	490000H-49FFFFH	248000H-247FFFH	6A0000H-6A1FFFH	3B1000H-3B1FFFH
40000H-4FFFFH	20000H-27FFFH	260000H-26FFFFH	130000H-137FFFH	480000H-48FFFFH	240000H-247FFFH	690000H-691FFFH	3B0000H-3B0FFFH
30000H-3FFFFH	18000H-17FFFH	250000H-25FFFFH	128000H-127FFFH	470000H-47FFFFH	238000H-237FFFH	680000H-681FFFH	3A0000H-3A0FFFH
20000H-2FFFFH	10000H-17FFFH	240000H-24FFFFH	120000H-127FFFH	460000H-46FFFFH	230000H-237FFFH	670000H-671FFFH	3A8000H-3A8FFFH
10000H-1FFFFH	08000H-07FFFH	230000H-23FFFFH	118000H-117FFFH	450000H-45FFFFH	228000H-227FFFH	660000H-661FFFH	3A7000H-3A7FFFH
00000H-0FFFFH	00000H-07FFFH	220000H-22FFFFH	110000H-117FFFH	440000H-44FFFFH	220000H-227FFFH	650000H-651FFFH	3A6000H-3A6FFFH
A21-A-1 (Byte Mode)	A21-A0 (Word Mode)	A21-A-1 (Byte Mode)	A21-A0 (Word Mode)	A21-A-1 (Byte Mode)	A21-A0 (Word Mode)	A21-A-1 (Byte Mode)	A21-A0 (Word Mode)

### Bus Operation

#### BYTE#=VIH

Mode \ Pins		CE#	OE#	WE#	RP#	DQ0-15
Read	Array	VIL	VIL	VIH	VIH	Data Output
	Status Register	VIL	VIL	VIH	VIH	Status Register Data
	Identifier Code	VIL	VIL	VIH	VIH	Identifier Code
	Page	VIL	VIL	VIH	VIH	Data Output
Output Disable		VIL	VIH	VIH	VIH	High-Z
Write	Program	VIL	VIH	VIL	VIH	Command/Data in
	Erase	VIL	VIH	VIL	VIH	Command
	Others	VIL	VIH	VIL	VIH	Command
Stand by		VIH	X <sup>1)</sup>	X <sup>1)</sup>	VIH	High-Z
Deep Power Down		X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	VIL	High-Z

#### BYTE#=VIL

Mode \ Pins		CE#	OE#	WE#	RP#	DQ0-7
Read	Array	VIL	VIL	VIH	VIH	Data Output
	Status Register	VIL	VIL	VIH	VIH	Status Register Data
	Identifier Code	VIL	VIL	VIH	VIH	Identifier Code
	Page	VIL	VIL	VIH	VIH	Data Output
Output Disable		VIL	VIH	VIH	VIH	High-Z
Write	Program	VIL	VIH	VIL	VIH	Command/Data in
	Erase	VIL	VIH	VIL	VIH	Command
	Others	VIL	VIH	VIL	VIH	Command
Stand by		VIH	X <sup>1)</sup>	X <sup>1)</sup>	VIH	High-Z
Deep Power Down		X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	VIL	High-Z

1) X can be VIH or VIL for control pins.

### Software Command Definition

#### Command List (WP# =VIH or VIL)

Command	1st Bus Cycle			2nd Bus Cycle			3rd-5th Bus Cycles			
	Mode	Address	Data <sup>1)</sup> (DQ0-15)	Mode	Address		Data (DQ0-15)	Mode	Address	Data (DQ0-15)
					A21-A18	A0				
Read Array	Write	X	FFH							
Page Read	Write	X	F3H	Read	SA <sup>5)</sup>		RD0 <sup>5)</sup>	Read	SA+i <sup>6)</sup>	RD <sub>i</sub> <sup>6)</sup>
Device Identifier	Write	Bank <sup>2)</sup>	90H	Read	Bank <sup>2)</sup>	IA <sup>3)</sup>	ID <sup>3)</sup>			
Read Status Register	Write	Bank <sup>2)</sup>	70H	Read	Bank <sup>2)</sup>		SRD <sup>4)</sup>			
Clear Status Register	Write	X	50H							
Suspend	Write	Bank <sup>2)</sup>	B0H							
Resume	Write	Bank <sup>2)</sup>	D0H							

- 1) In the case of Word mode(BYTE#=VIH), upper byte data (DQ15-DQ8) is ignored.
- 2) IA=ID code address: A0=VIL (Manufacturer's code): A0=VIH (Device code), ID=ID code
- 3) Bank=Bank address (Bank(I)-Bank(IV): A21-18)
- 4) SRD=Status Register Data
- 5) SA=A21-A2:1<sup>st</sup> Page Address, A1,A0:voluntary address / RD0=1<sup>st</sup> Page read data
- 6) SA+i: Page address(is equal to 1<sup>st</sup> Page Address of A21-A2), A1,A0: voluntary address / RD<sub>i</sub>:  
2<sup>nd</sup> Page read data

#### Command List (WP# =VIH)

Command	1st Bus Cycle			2nd Bus Cycle			3rd-129th Bus Cycles (Word mode) 3rd-257th Bus Cycles (Byte mode)		
	Mode	Address	Data <sup>1)</sup> (DQ0-15),(DQ0-7)	Mode	Address	Data <sup>1)</sup> (DQ0-15),(DQ0-7)	Mode	Address	Data <sup>1)</sup> (DQ0-15),(DQ0-7)
Word/Byte Program	Write	Bank <sup>2)</sup>	40H	Write	WA <sup>3)</sup>	WD <sup>3)</sup>			
Page Program	Write	Bank <sup>2)</sup>	41H	Write	WA0 <sup>4)</sup>	WD0 <sup>4)</sup>	Write	WAn <sup>4)</sup>	WDn <sup>4)</sup>
Page Buffer to Flash	Write	Bank <sup>2)</sup>	0EH	Write	WA <sup>5)</sup>	D0H <sup>1)</sup>			
Block Erase/Confirm	Write	Bank <sup>2)</sup>	20H	Write	BA <sup>6)</sup>	D0H <sup>1)</sup>			
Erase All Unlocked Blocks	Write	X	A7H	Write	X	D0H <sup>1)</sup>			
Clear Page Buffer	Write	X	55H	Write	X	D0H <sup>1)</sup>			
Single Data Load to Page Buffer	Write	X	74H	Write	WA <sup>3)</sup>	WD <sup>3)</sup>			
Flash to Page Buffer	Write	Bank <sup>2)</sup>	F1H	Write	RA <sup>7)</sup>	D0H <sup>1)</sup>			

- 1) In the case of Word mode(BYTE#=VIH),Upper byte data (DQ15-DQ8) is ignored.
- 2) Bank=Bank address (Bank(I)-Bank(IV): A21-A18)
- 3) WA=Write Address, WD=Write Data
- 4) WA0, WAn=Write Address, WD0, WDn=Write Data.  
Word mode (BYTE#=VIH) : Write address and write data must be provided sequentially from 00H to 7FH for A6-A0.  
Page size is 128 words (128-word x 16-bit), and also A21-A7 (block address, page address) must be valid.  
Byte mode (BYTE#=VIL) : Write address and write data must be provided sequentially from 00H to FFH for A6-A-1.  
Page size is 256 Bytes (256-byte x 8-bit), and also A21-A7 (block address, page address) must be valid.
- 5) WA=Write Address: A21-A7 (block address, page address) must be valid.
- 6) BA=Block Address : A21-A12[Bank(I)], A21-A15 [Bank(II), Bank(III), Bank(IV)] must be valid.
- 7) RA=Read Address: A21-A7 (block address, page address) must be valid.

### Software Command Definition Command List (WP# =VIL)

Software lock release operation needs following consecutive 7bus cycles. Moreover, additional 127(255) bus cycles are needed for page program operation.

Setup Command for Software Lock Release	1st Bus Cycle			2nd Bus Cycle			3rd Bus Cycle		
	Mode	Address	Data <sup>1)</sup> (DQ0-15/DQ0-7)	Mode	Address	Data <sup>1)</sup> (DQ0-15/DQ0-7)	Mode	Address	Data <sup>1)</sup> (DQ0-15/DQ0-7)
Word/Byte Program	Write	Bank	60H	Write	Bank	Block <sup>6)</sup>	Write	Bank	ACH
Page Program	Write	Bank	60H	Write	Bank	Block <sup>6)</sup>	Write	Bank	ACH
Page Buffer to Flash	Write	Bank	60H	Write	Bank	Block <sup>6)</sup>	Write	Bank	ACH
Block Erase/Confirm	Write	Bank	60H	Write	Bank	Block <sup>6)</sup>	Write	Bank	ACH
Clear Page Buffer	Write	Bank	60H	Write	Bank	Block <sup>6)</sup>	Write	Bank	ACH
Single Data Load to Page Buffer	Write	Bank	60H	Write	Bank	Block <sup>6)</sup>	Write	Bank	ACH
Flash to Page Buffer	Write	Bank	60H	Write	Bank	Block <sup>6)</sup>	Write	Bank	ACH

Setup Command for Software Lock Release	4th Bus Cycle			5th Bus Cycle		
	Mode	Address	Data <sup>1)</sup> (DQ0-15/DQ0-7)	Mode	Address	Data <sup>1)</sup> (DQ0-15/DQ0-7)
Word/Byte Program	Write	Bank	Block# <sup>6)</sup>	Write	Bank	7BH
Page Program	Write	Bank	Block# <sup>6)</sup>	Write	Bank	7BH
Page Buffer to Flash	Write	Bank	Block# <sup>6)</sup>	Write	Bank	7BH
Block Erase/Confirm	Write	Bank	Block# <sup>6)</sup>	Write	Bank	7BH
Clear Page Buffer	Write	Bank	Block# <sup>6)</sup>	Write	Bank	7BH
Single Data Load to Page Buffer	Write	Bank	Block# <sup>6)</sup>	Write	Bank	7BH
Flash to Page Buffer	Write	Bank	Block# <sup>6)</sup>	Write	Bank	7BH

Setup Command for Program or Erase Operations	6th Bus Cycle			7th Bus Cycle			8th-134th Bus Cycles(Word mode) 8th-262th Bus Cycles(Byte mode)		
	Mode	Address	Data <sup>1)</sup> (DQ0-15/DQ0-7)	Mode	Address	Data (DQ0-15/DQ0-7)	Mode	Address	Data (DQ0-15/DQ0-7)
Word/Byte Program	Write	Bank	40H	Write	WA <sup>2)</sup>	WD <sup>2)</sup>			
Page Program	Write	Bank	41H	Write	WA0 <sup>3)</sup>	WD0 <sup>3)</sup>	Write	WAn <sup>3)</sup>	WDn <sup>3)</sup>
Page Buffer to Flash	Write	Bank	0EH	Write	WA <sup>4)</sup>	D0H <sup>1)</sup>			
Block Erase/Confirm	Write	Bank	20H	Write	BA <sup>5)</sup>	D0H <sup>1)</sup>			
Clear Page Buffer	Write	X	55H	Write	X	D0H <sup>1)</sup>			
Single Data Load to Page Buffer	Write	X	74H	Write	WA <sup>2)</sup>	WD <sup>2)</sup>			
Flash to Page Buffer	Write	Bank	F1H	Write	RA <sup>7)</sup>	D0H <sup>1)</sup>			

1) In the case of word mode(BYTE#=VIH) upper byte data (DQ15-DQ8) is ignored.

2) WA=Write Address, WD=Write Data

3) WA0, WAn=Write Address, WD0, WDn=Write Data. Write address and write data must be provided sequentially from 00H to 7FH for A6-A0(word mode) and from 00H to FFH for A6-A-1(byte mode), respectively.

Page size is 128 words (128-word x 16-bit/ word mode) or Page size is 256 bytes (256-word x 8-bit/ byte mode), and also A21-A7 (block address, page address) must be valid.

4) WA=Write Address: A21-A7 (block address, page address) must be valid.

5) BA=Block Address : A21-A12[Bank(I)], A21-A15 [Bank(II), Bank(III), Bank(IV)]

6) Block=Block Address: A21-A15, Block#=A21#-A15# must be valid.

Address	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Block	fixed 0	A21	A20	A19	A18	A17	A16	A15
Block#	fixed 0	A21#	A20#	A19#	A18#	A17#	A16#	A15#

7) RA=Read Address: A21-A7 (block address, page address) must be valid.

# Preliminary

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Renesas LSIs

## M5M29KB/T641ATP

67,108,864-BIT (8,388,608-WORD BY 8-BIT /4,194,304-WORD BY 16-BIT)  
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

### Block Locking

RP#	WP#	Write Protection Provided					Notes
		Bank(I)		Bank(II)	Bank(III)	Bank(IV)	
		Boot	Parameter/Main	Main	Main	Main	
VIL	X	Locked	Locked	Locked	Locked	Locked	Deep Power Down Mode
VIH	VIL	Locked	Locked	Locked	Locked	Locked	All Blocks Locked(Valid to operate Software Lock Release)
	VIH	Unlocked	Unlocked	Unlocked	Unlocked	Unlocked	All Blocks Unlocked

WP# pin must not be switched during performing Read / Write operations or WSM busy (WSMS=0).

### Status Register

Symbol (I/O Pin)	Status	Definition	
		"1"	"0"
S.R. 7 (DQ7)	Write State Machine Status	Ready	Busy
S.R. 6 (DQ6)	Suspend Status	Suspended	Operation in Progress/Completed
S.R. 5 (DQ5)	Erase Status	Error	Successful
S.R. 4 (DQ4)	Program Status	Error	Successful
S.R. 3 (DQ3)	Block Status after Erase	Error	Successful
S.R. 2 (DQ2)	Reserved	-	-
S.R. 1 (DQ1)	Reserved	-	-
S.R. 0 (DQ0)	Reserved	-	-

### Device ID Code

Code \ Pins	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Hex. Data
Manufacturer Code	VIL	"0"	"0"	"0"	"1"	"1"	"1"	"0"	"0"	1CH
Device Code (Top Boot)	VIH	"1"	"0"	"1"	"1"	"1"	"0"	"0"	"0"	B8H
Device Code (Bottom Boot)	VIH	"1"	"0"	"1"	"1"	"1"	"0"	"0"	"1"	B9H

In the case of word mode, The output of upper byte data (DQ15-DQ8) is "0H".

### Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min.	Max.	Units
VCC	VCC Voltage	With Respect to GND	-0.2	4.6	V
VI1	All Input or Output Voltage <sup>1)</sup>		-0.6	4.6	V
Ta	Ambient Temperature		-40	85	°C
Tbs	Temperature under Bias		-50	95	°C
Tstg	Storage Temperature		-65	125	°C
Iout	Output Short Circuit Current			100	mA

<sup>1)</sup>Minimum DC voltage is -0.5V on input / output pins. During transitions, the level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input / output pins is VCC+0.5V which, during transitions, may overshoot to VCC+1.5V for periods <20ns.

### DC electrical characteristics

(Ta= -40 ~85 °C and Flash VCC=3.0V~3.6V, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits			Units
			Min.	Typ. <sup>1)</sup>	Max.	
ILI	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$	-1.0		+1.0	μA
ILO	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$	-10		+10	μA
ISB2	VCC Stand by Current	VCC= 3.6V, VIN= GND/VCC, CE#= RP#= VCC ±0.3V		0.1	6	μA
ISB3	VCC Deep Power Down Current	VCC= 3.6V, VIN= VIL/VIH, RP#= VIL		5	25	μA
ISB4		VCC= 3.6V, VIN= GND or VCC, RP#= GND±0.3V		0.1	6	μA
ICC1	VCC Read Current for Word / byte	Vcc = 3.6V, VIN = VIL/VIH, RP# = OE# = WE# = VIH, CE# = VIL, Iout = 0mA	5MHz	20	30	mA
			1MHz	4	8	mA
ICC1P	VCC Page Read Current	Vcc = 3.6V, VIN = VIL/VIH, RP# = OE# = VIH, CE# = VIL, Iout = 0mA	5MHz	5	10	mA
ICC2	VCC Write Current for Word / byte	Vcc = 3.6V, VIN = VIL/VIH, RP# = OE# = VIH, CE# = WE# = VIL			15	mA
ICC3	VCC Program Current	VCC = 3.6V, VIN = VIL/VIH, CE#= RP# = VIH			35	mA
ICC4	VCC Erase Current	VCC = 3.6V, VIN = VIL/VIH, CE#= RP# = VIH			35	mA
ICC5	VCC Suspend Current	VCC = 3.6V, VIN = VIL/VIH, CE#= RP# = VIH			200	μA
VIL	Input Low Voltage		-0.5		0.4	V
VIH	Input High Voltage		2.4		VCC+0.5	V
VOL	Output Low Voltage	IOL = 4.0mA			0.45	V
VOH1	Output High Voltage	IOH = -2.0mA	0.85xVCC			V
VOH2		IOH = -100uA	VCC-0.4			V
VLKO	Low VCC Lock Out Voltage <sup>2)</sup>		1.5		2.2	V

All currents are in RMS unless otherwise noted.

1) Typical values at Flash VCC=3.3V, Ta=25 °C.

2) To protect against initiation of write cycle during Flash VCC power up / down, a write cycle is locked out for Flash VCC less than VLKO. If Flash VCC is less than VLKO, Write State Machine is reset to read mode. When the Write State Machine is in Busy state, if Flash VCC is less than VLKO, the alteration of memory contents may occur.

# Preliminary

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Renesas LSIs

## M5M29KB/T641ATP

67,108,864-BIT (8,388,608-WORD BY 8-BIT /4,194,304-WORD BY 16-BIT)  
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

### AC electrical characteristics (Ta=-40 ~85 °C and Flash VCC=3.0V~3.6V, unless otherwise noted)

#### Read Only Mode

Symbol		Parameter	Limits			Units
			Flash VCC=3.0-3.6V			
			Min.	Typ.	Max.	
tRC	tAVAV	Read Cycle Time	70			ns
ta(AD)	tAVQV	Address Access Time			70	ns
ta(CE)	tELQV	Chip Enable Access Time			70	ns
ta(OE)	tGLQV	Output Enable Access Time			30	ns
ta(PAD)	tPAVQV	Page Read Access Time			25	ns
tCEPH		CE# "H" Pulse width	30			ns
tCLZ	tELQX	Chip Enable to Output in Low-Z	0			ns
tDF(CE)	tEHQZ	Chip Enable High to Output in High-Z			25	ns
tOLZ	tGLQX	Output Enable to Output in Low-Z	0			ns
tDF(OE)	tGHQZ	Output Enable to High to Output in High-Z			25	ns
tPHZ	tPLQZ	RP# Low to Output High-Z			150	ns
ta(BYTE)	tFL/HQV	BYTE# access time			70	ns
tBHZ	tFLQZ	BYTE# low to output high-Z			25	ns
tOH	tOH	Output Hold from CE#, OE# and Address	0			ns
tBCD	tELFL/H	CE# low to BYTE# high or low			5	ns
tBAD	tAVFL/H	Address to BYTE# high or low			5	ns
tOEH	tWHGL	OE# Hold from WE# High	10			ns
tPS	tPHEL	RP# Recovery to CE# Low	150			ns

-Timing measurements are made under AC waveforms for read operations.

# Preliminary

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Renesas LSIs

## M5M29KB/T641ATP

67,108,864-BIT (8,388,608-WORD BY 8-BIT /4,194,304-WORD BY 16-BIT)  
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

### AC electrical characteristics (Ta=-40 ~85 °C and Flash VCC=3.0V~3.6V, unless otherwise noted)

#### Read / Write Mode (WE# control)

Symbol	Parameter	Limits			Units	
		Flash VCC=3.0-3.6V				
		Min.	Typ.	Max.		
tWC	tAVAV	Write Cycle Time	70		ns	
tAS	tAVWH	Address Setup Time	35		ns	
tAH	tWHAX	Address Hold Time	0		ns	
tDS	tDVWH	Data Setup Time	35		ns	
tDH	tWHDX	Data Hold Time	0		ns	
tOE#H	tWHGL	OE# Hold from WE# High	10		ns	
tCS	tELWL	Chip Enable Setup Time	0		ns	
tCH	tWHEH	Chip Enable Hold Time	0		ns	
tWP	tWLWH	Write Pulse Width	35		ns	
tWPH	tWHWL	Write Pulse Width High	30		ns	
tBS	tFL/HWH	Byte enable high or low set-up time	50		ns	
tBH	tWFL/H	Byte enable high or low hold time	70		ns	
tGHWL	tGHWL	OE# Hold to WE# Low	0		ns	
tBLS	tPHHWH	Block Lock Setup to Write Enable High	70		ns	
tBLH	tQVPH	Block Lock Hold from Valid SRD	0		ns	
tDAP	tWHRH1	Duration of Auto Program Operation(Byte Mode)		30	300	µs
tDAP	tWHRH1	Duration of Auto Program Operation(Word Mode)		30	300	µs
tDAP	tWHRH1	Duration of Auto Program Operation(Page Mode)		4	80	ms
tDAE	tWHRH2	Duration of Auto Block Erase Operation		150	600	ms
tWHRL	tWHRL	Delay Time During Internal Operation			70	ns
tPS	tPHWL	RP# Recovery to WE# Low	150			ns

-Read timing parameters during command write operations mode are the same as during read only operation mode.

-Typical values at Flash VCC=3.3V and Ta=25 °C.

#### Read / Write Mode (CE# control)

Symbol	Parameter	Limits			Units	
		Flash VCC=3.0-3.6V				
		Min.	Typ.	Max.		
tWC	tAVAV	Write Cycle Time	70		ns	
tAS	tAVEH	Address Setup Time	35		ns	
tAH	tEHAX	Address Hold Time	0		ns	
tDS	tDVEH	Data Setup Time	35		ns	
tDH	tEHDX	Data Hold Time	0		ns	
tOE#H	tEHGL	OE# Hold from CE# High	10		ns	
tWS	tWLEL	Write Enable Setup Time	0		ns	
tWH	tEHWH	Write Enable Hold Time	0		ns	
tCEP	tELEH	CE# Pulse Width	35		ns	
tCEPH	tEHEL	CE#"H" Pulse Width	30		ns	
tBS	tFL/HEH	Byte enable high or low set-up time	50		ns	
tBH	tEHFL/H	Byte enable high or low hold time	70		ns	
tGHLEL	tGHLEL	OE# Hold to CE# Low	0		ns	
tBLS	tPHHEH	Block Lock Setup to Chip Enable High	70		ns	
tBLH	tQVPH	Block Lock Hold from Valid SRD	0		ns	
tDAP	tEHRH1	Duration of Auto Program Operation(Byte Mode)		30	300	µs
tDAP	tEHRH1	Duration of Auto Program Operation(Word Mode)		30	300	µs
tDAP	tEHRH1	Duration of Auto Program Operation(Page Mode)		4	80	ms
tDAE	tEHRH2	Duration of Auto Block Erase Operation		150	600	ms
tEHL	tEHL	Delay Time During Internal Operation			70	ns
tPS	tPEL	RP# Recovery to CE# Low	150			ns

-Timing measurements are made under AC waveforms for read operations.

-Typical values at Flash VCC=3.3V and Ta=25 °C.



### Program / Erase Time

Parameter	Min.	Typ.	Max.	Units
Block Erase Time		150	600	ms
Main Block Write Time (Byte Mode)		2	8	sec
Main Block Write Time (Word Mode)		1	4	sec
Page Write Time		4	80	ms
Flash to Page Buffer Time		100	150	μs

### Program Suspend / Erase Suspend Time

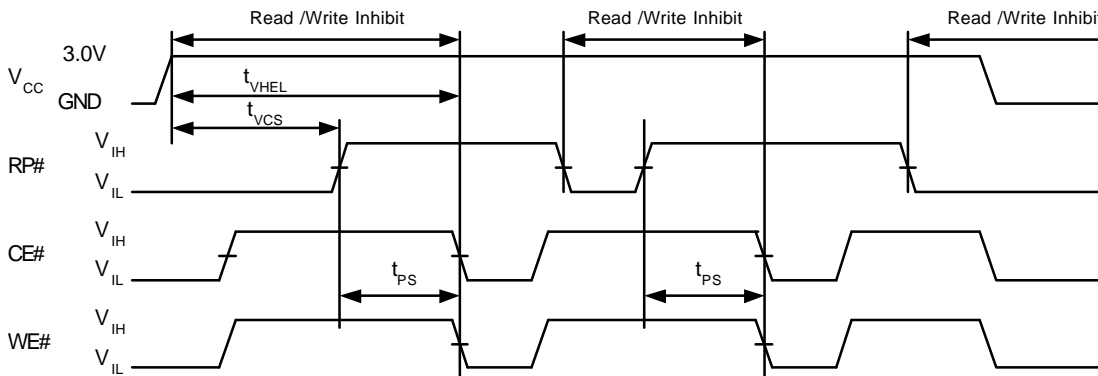
Parameter	Min.	Typ.	Max.	Unit
Program Suspend Time			15	μs
Erase Suspend Time			15	μs

### Flash VCC Power Up / Down Timing

symbol	Parameter	Min.	Typ.	Max.	Unit
tVCS	RP#=VIH Setup Time from Flash VCC min.	2			μs
tVHEL	CE#=VIL Setup Time from Flash VCC min.	60			μs

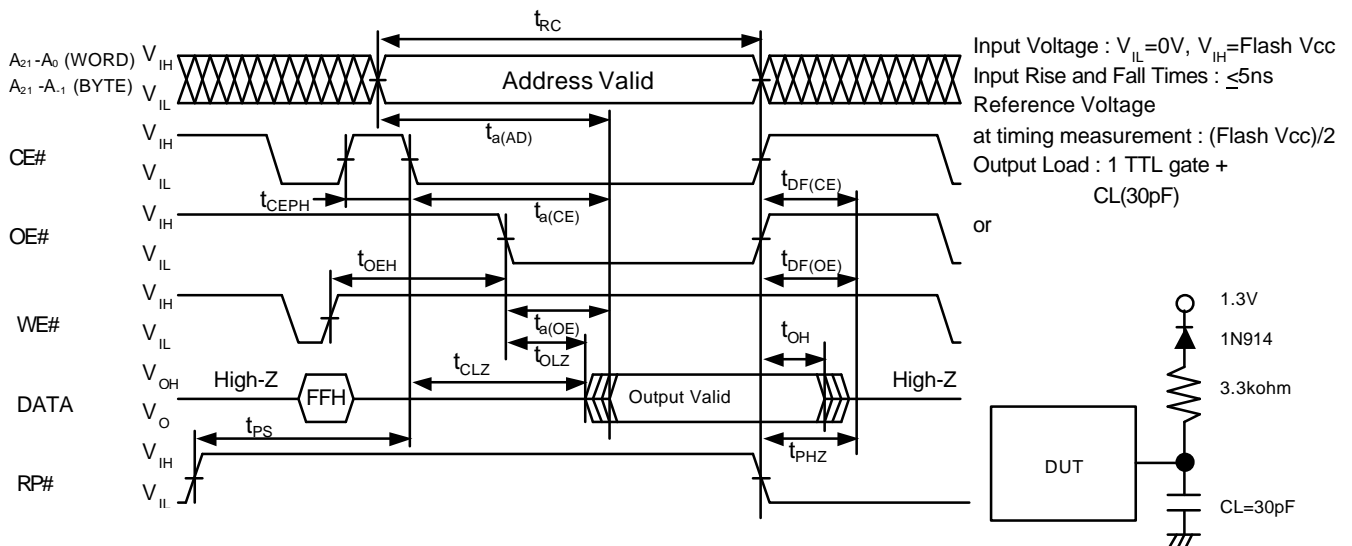
During power up / down, by the noise pulses on control pins, the device has possibility of accidental erase of programming. The device must be protected against initiation of write cycle for memory contents during power up / down. The delay time of min. 60 μsec is always required before read operation or write operation is initiated from the time Flash VCC reaches Flash VCC min. during power up /down. By holding RP#=VIL, the contents of memory is protected during Flash VCC power up / down. During power up, RP# must be held VIL for min. 2μs from the time Flash VCC reaches Flash VCC min.. During power down, RP# must be held VIL until Flash VCC reaches GND. RP# doesn't have latch mode, therefore RP# must be held VIH during read operation or erase / program operation.

### Flash VCC Power up / down Timing



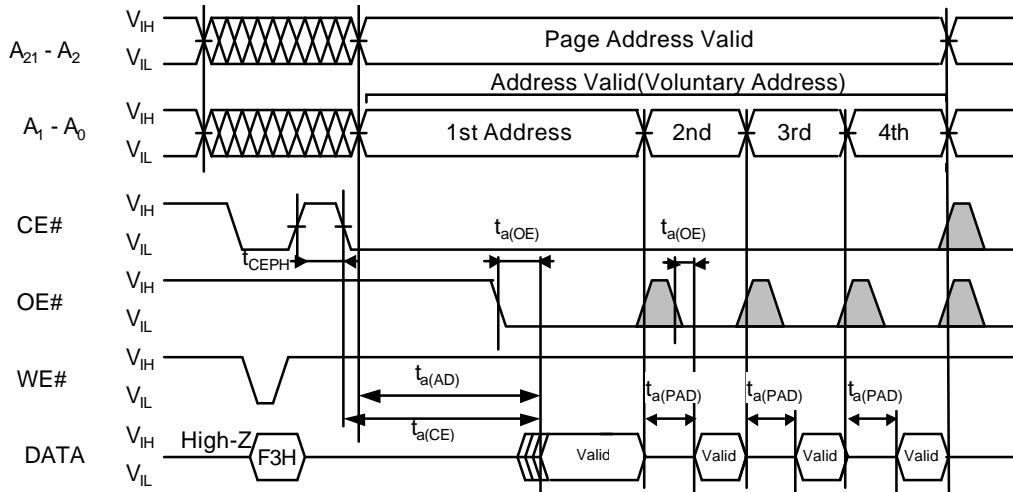
### AC Waveforms for Read Operation and Test Conditions

### Test Conditions for AC Characteristics



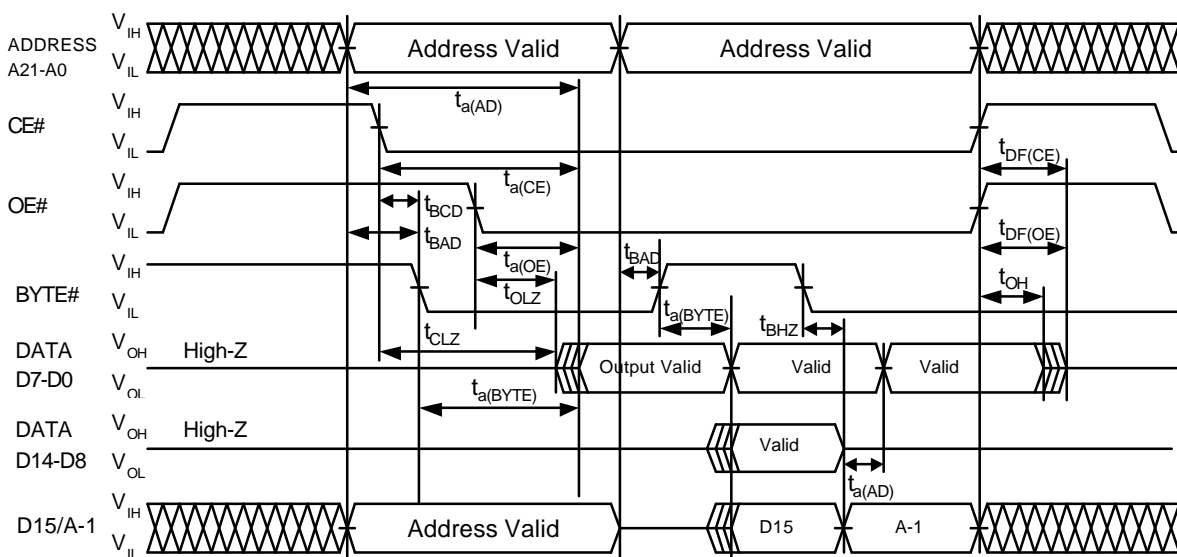
- After inputting Read Array Command FFH, it is necessary to make CE# "H" pulse more than 30ns (t<sub>CEPH</sub>). And after inputting Read Array Command FFH, it is also necessary to keep 30ns to recover before starting read after WE# rises "H" in case of changing a part or all of addresses( A<sub>21</sub>~A<sub>0</sub>/A<sub>21</sub>~A<sub>1</sub>) and CE#="L".

### AC waveforms for Page Read Operation



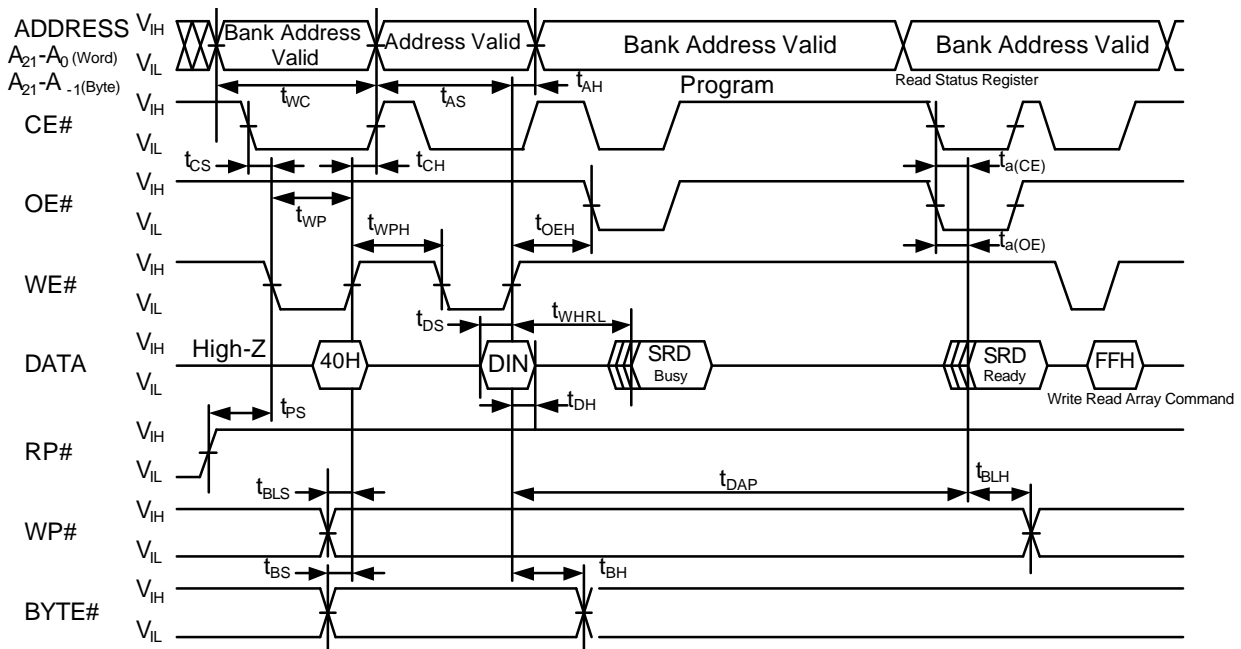
- After inputting Page Read Command F3H, it is necessary to make CE# "H" pulse more than 30ns ( $t_{CEPH}$ ).  
And after inputting Page Read Command F3H, it is also necessary to keep 30ns to recover before starting read after WE# rises "H" in case of changing address(es) and CE#="L".
- Once Page Read mode is valid, the mode is kept until RP# is set to VIL or the chip is powered off.

### Word/Byte AC Waveforms for Read Operation

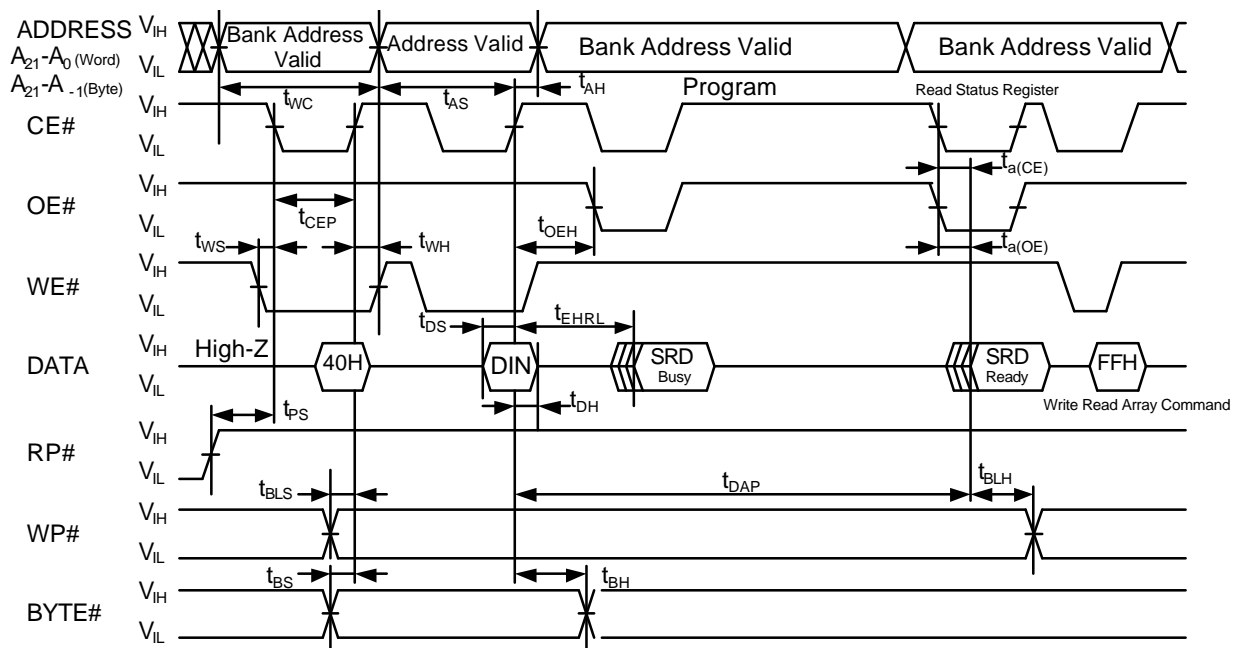


When BYTE# = VIH, CE# = OE# = VIL, D15/A-1 is output status. At this time, input signal must not be applied.

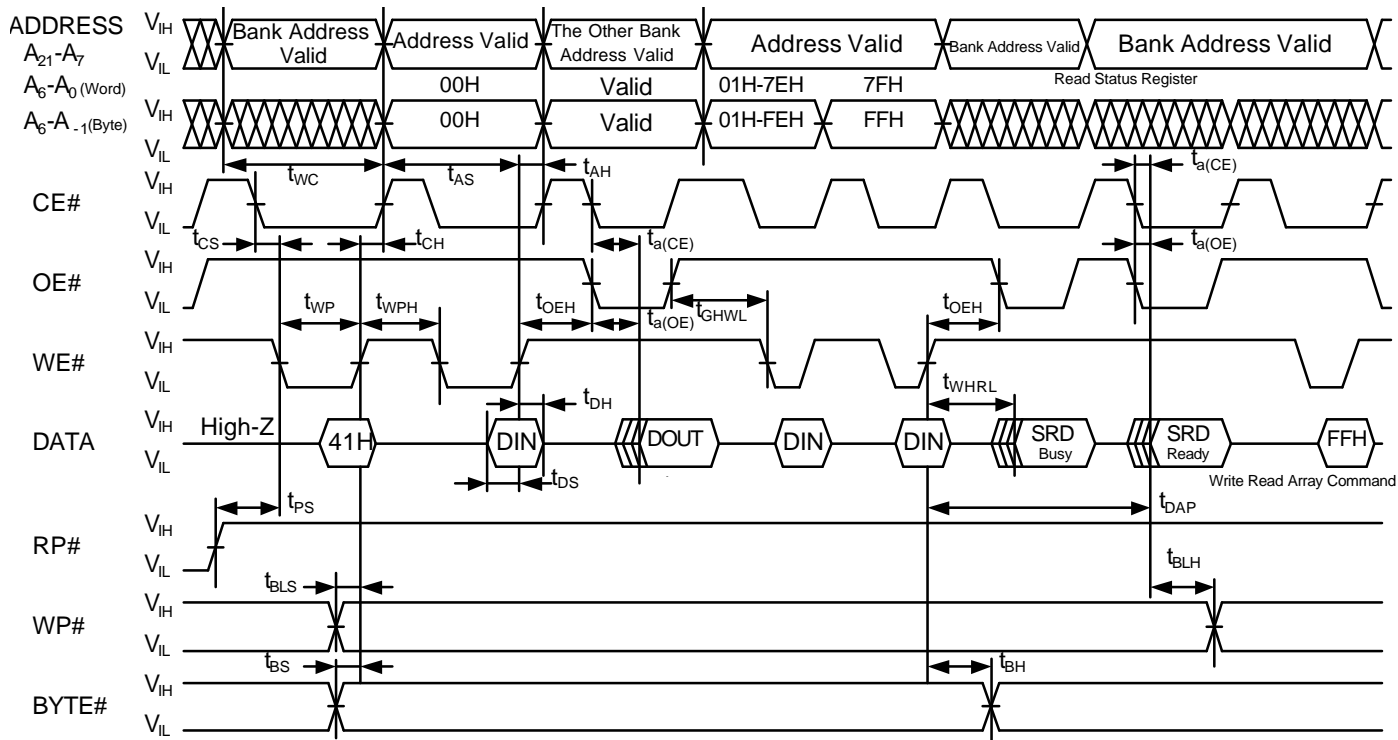
### AC Waveforms for Word / Byte Program Operation (WE# Control)



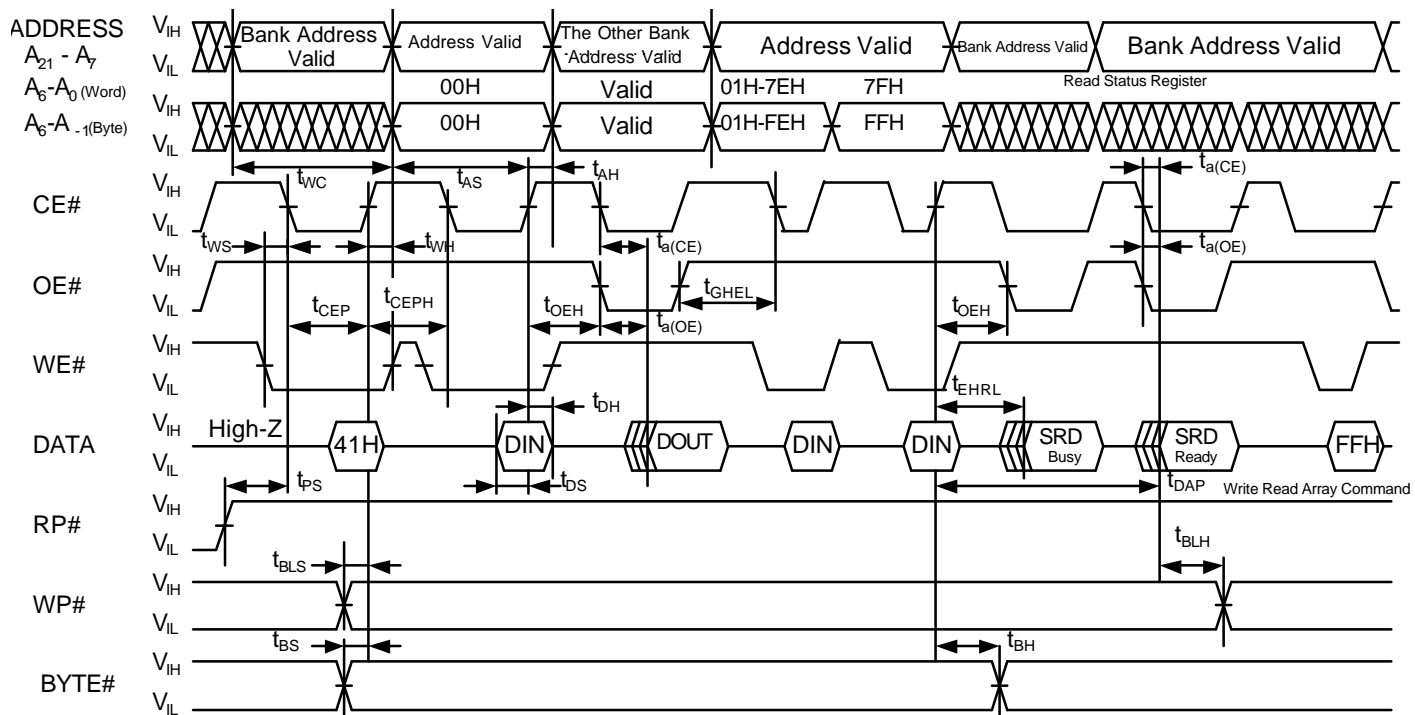
### AC Waveforms for Word / Byte Program Operation (CE# Control)



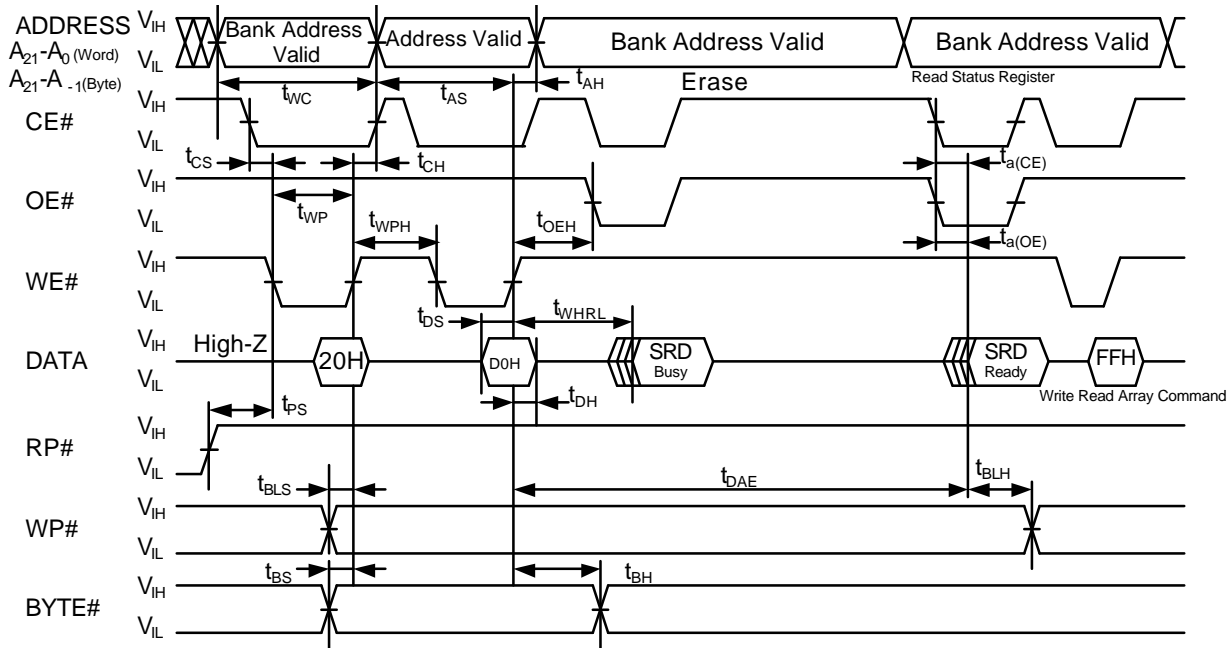
### AC Waveforms for Page Program Operation (WE# Control)



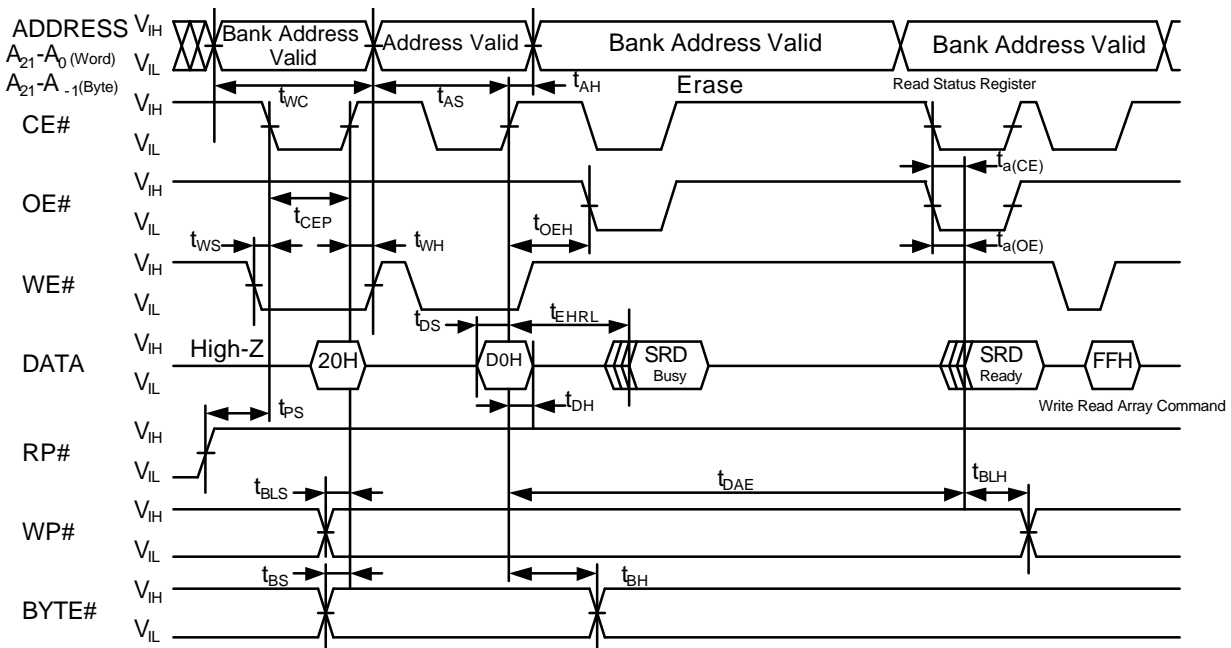
### AC Waveforms for Page Program Operation (CE# Control)



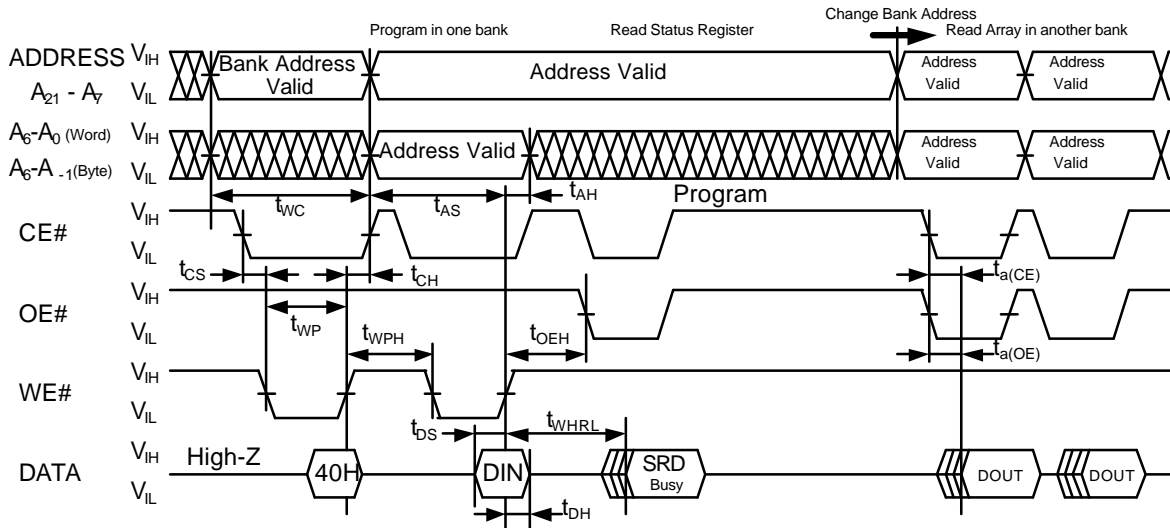
### AC Waveforms for Erase Operation (WE# Control)



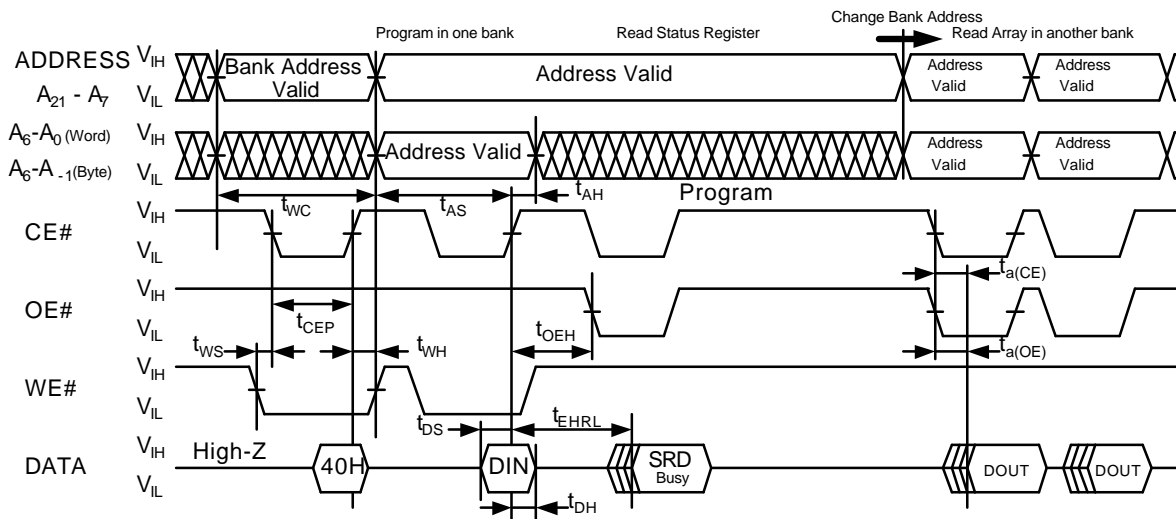
### AC Waveforms for Erase Operation (CE# Control)



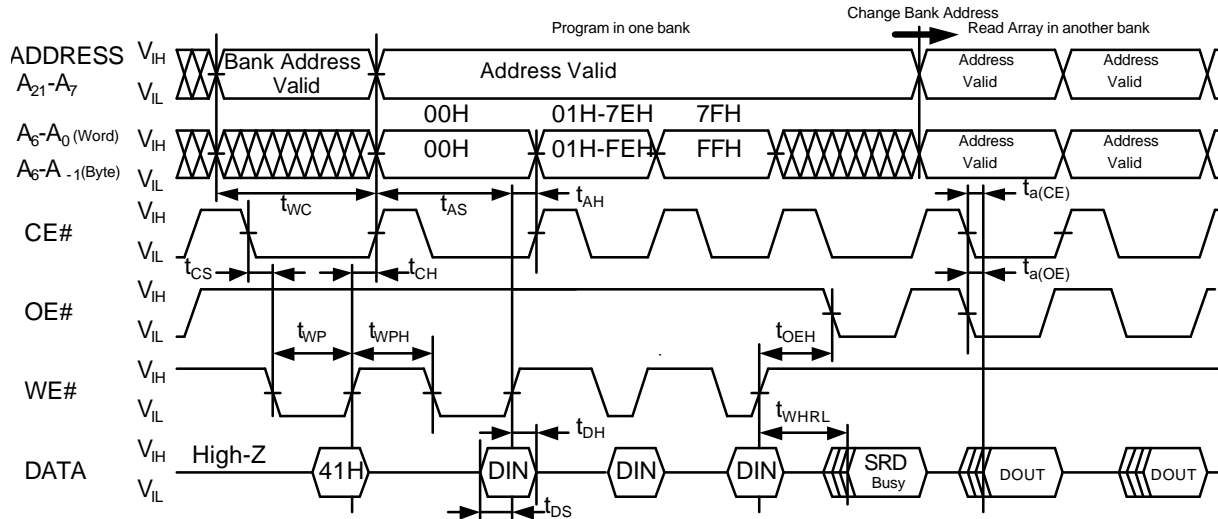
### AC Waveforms for Word / Byte Program Operation with BGO (WE# Control)



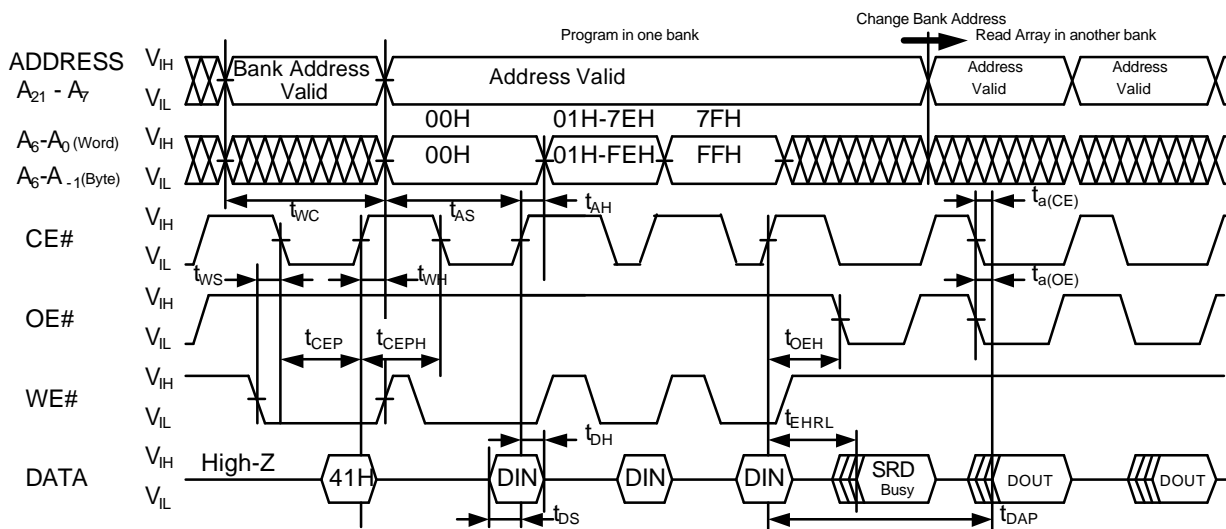
### AC Waveforms for Word / Byte Program Operation with BGO (CE# Control)



### AC Waveforms for Page Program Operation with BGO (WE# Control)

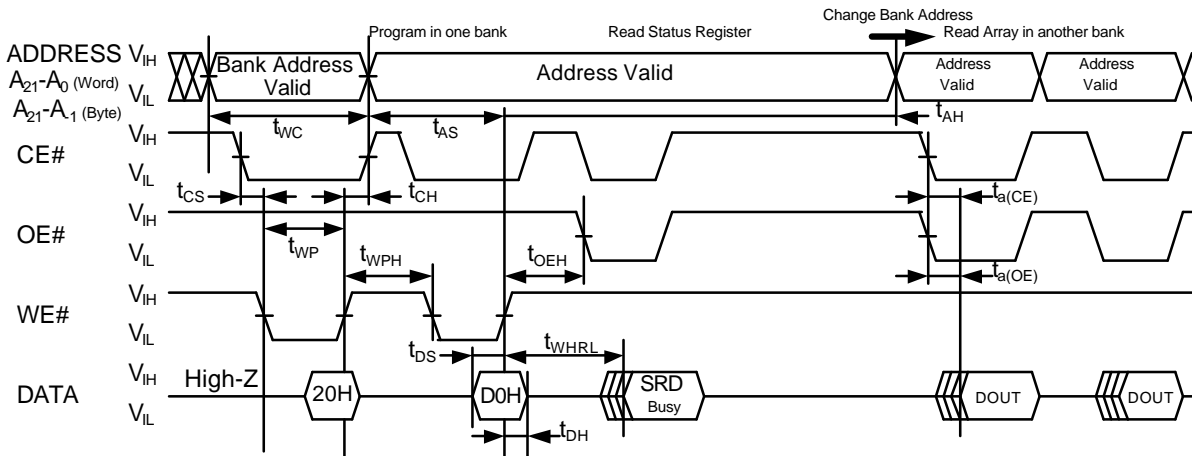


### AC Waveforms for Page Program Operation with BGO (CE# Control)

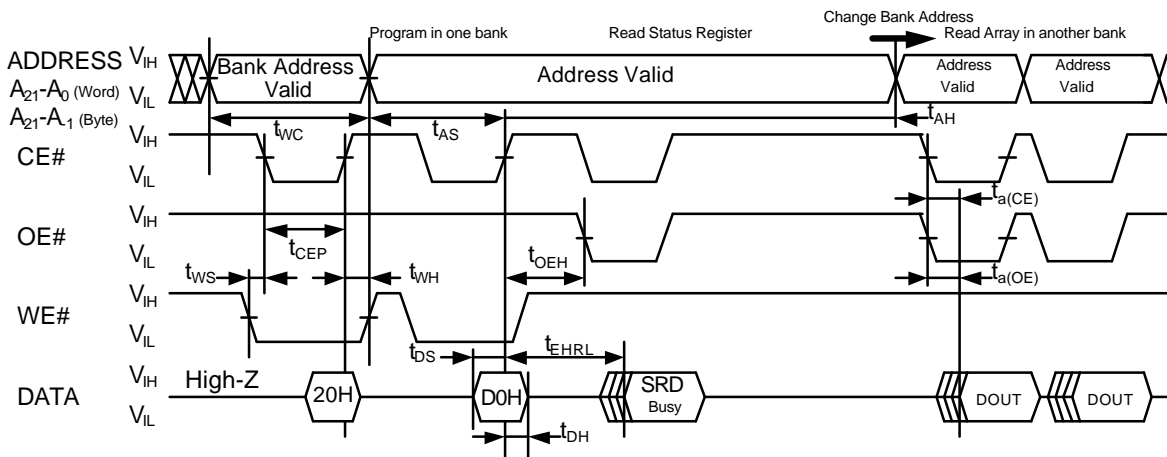




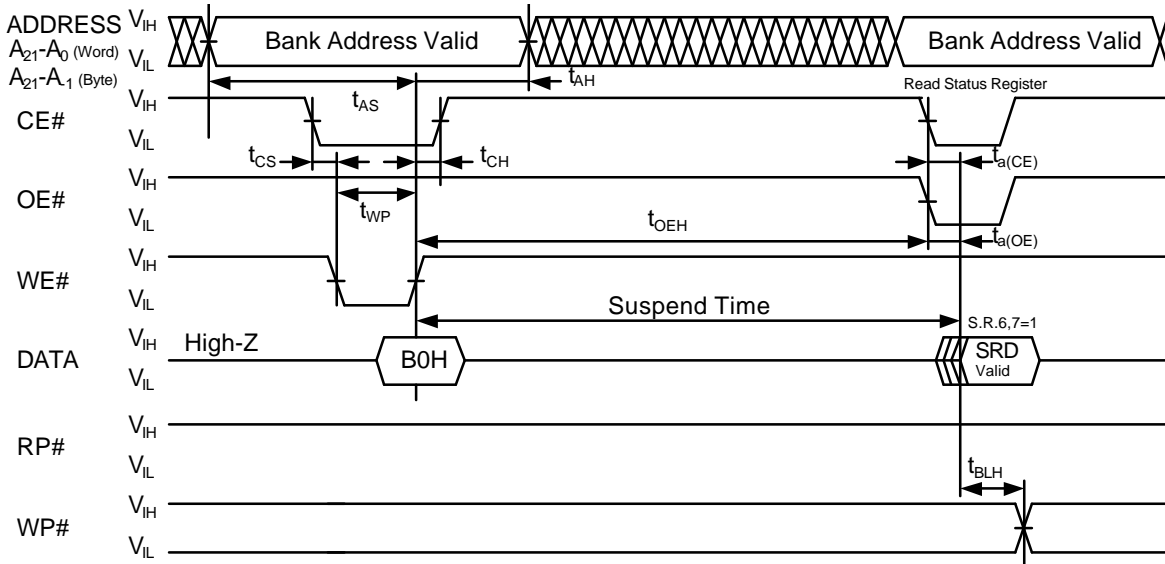
### AC Waveforms for Erase Operation with BGO (WE# Control)



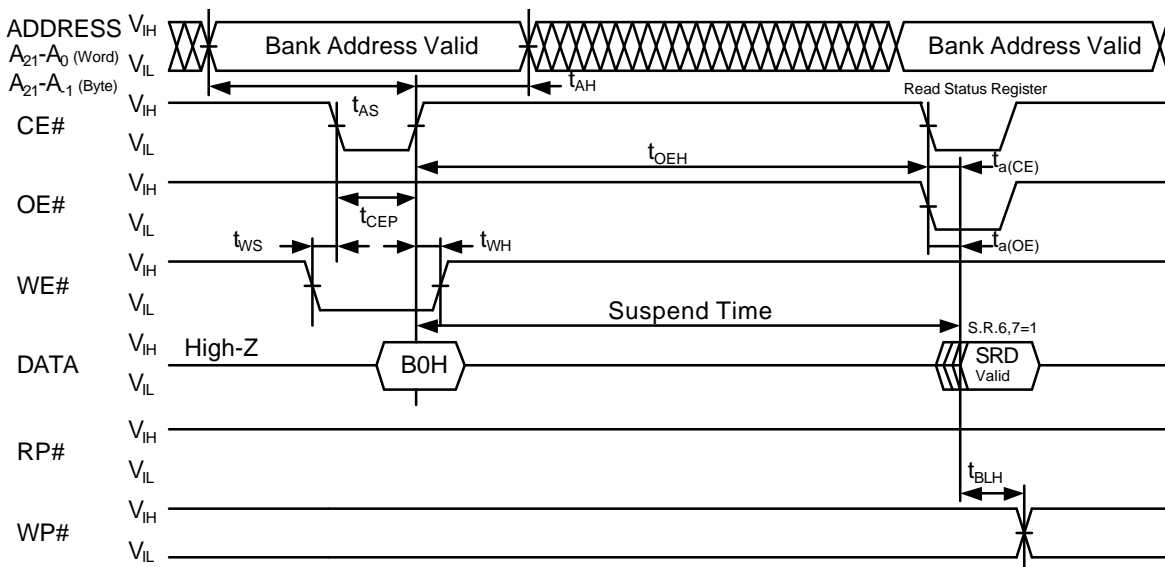
### AC Waveforms for Erase Operation with BGO (CE# Control)



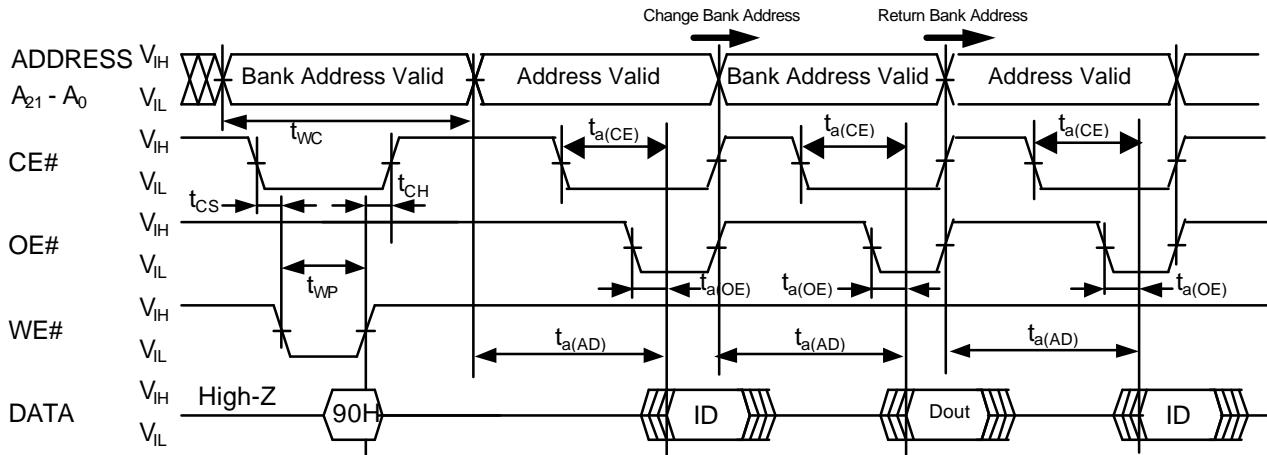
### AC Waveforms for Suspend Operation (WE# Control)



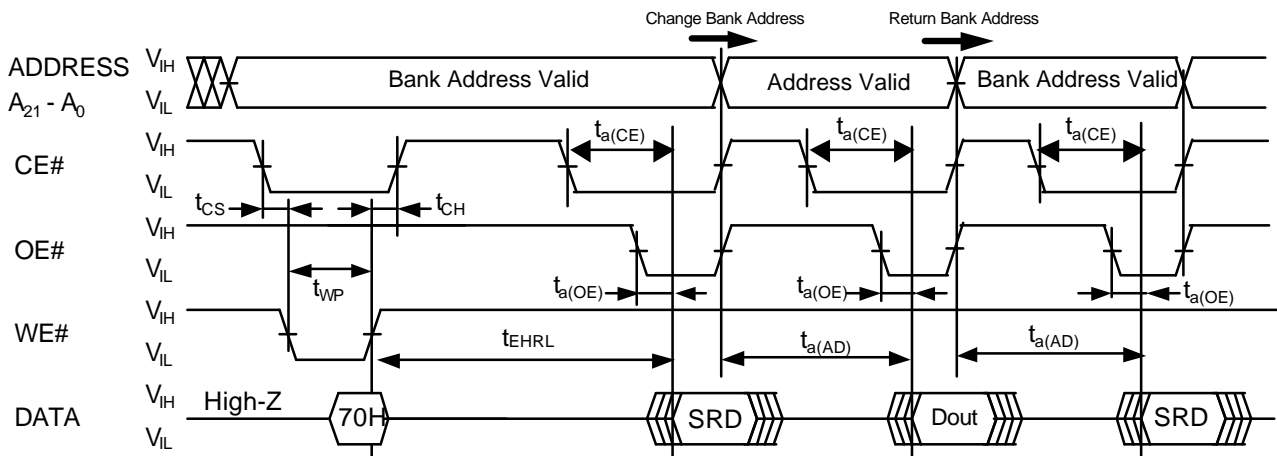
### AC Waveforms for Suspend Operation (CE# Control)



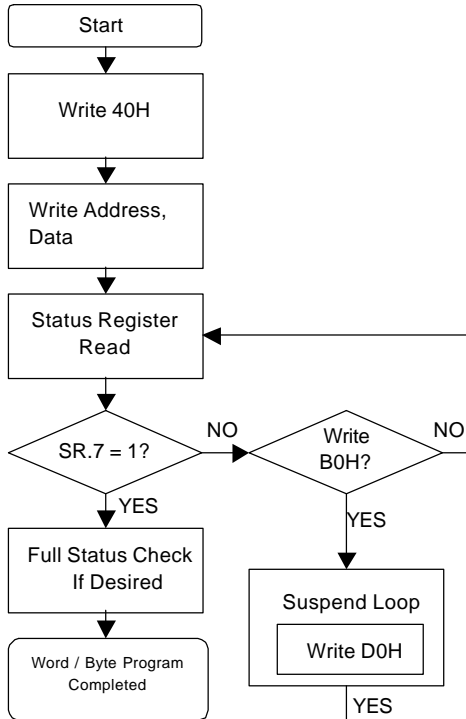
### AC Waveforms for Device ID Read Operation with BBR(Back Bank Read)



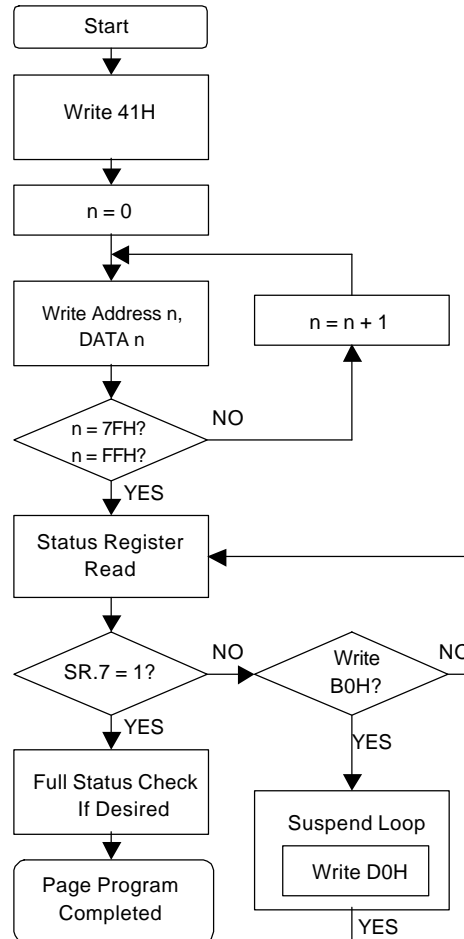
### AC Waveforms for Status Register Read Operation with BBR(Back Bank Read)



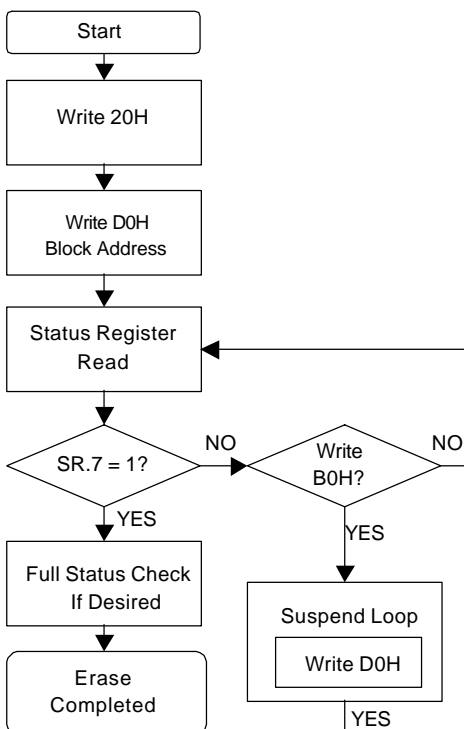
### Word / Byte Program Flow Chart



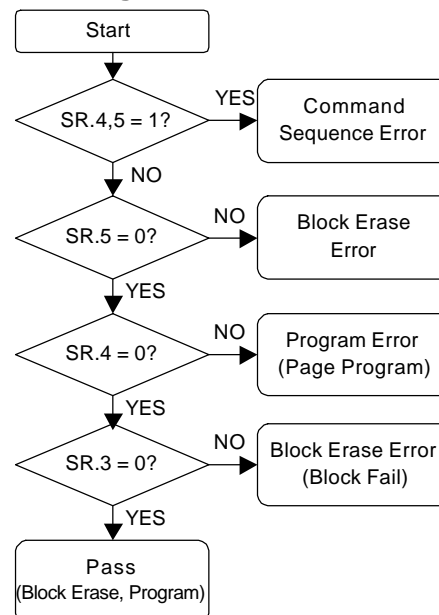
### Page Program Flow Chart



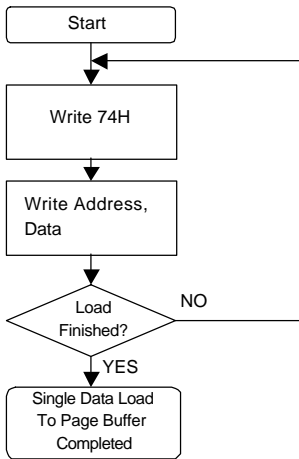
### Block Erase Flow Chart



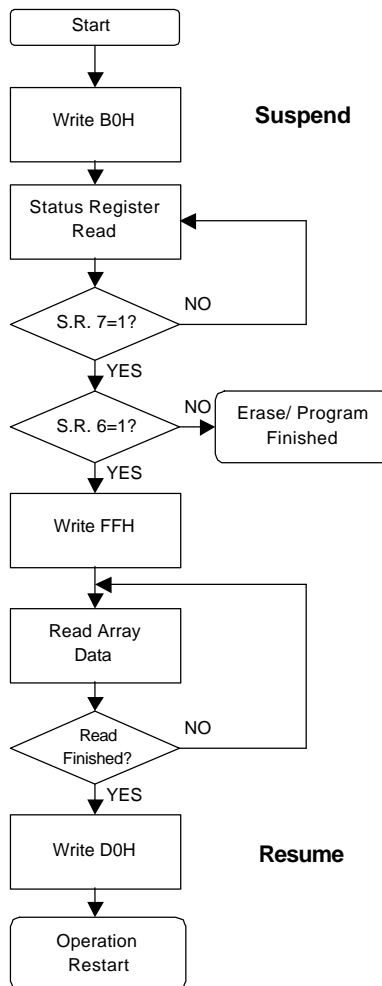
### Status Register Check Flow Chart



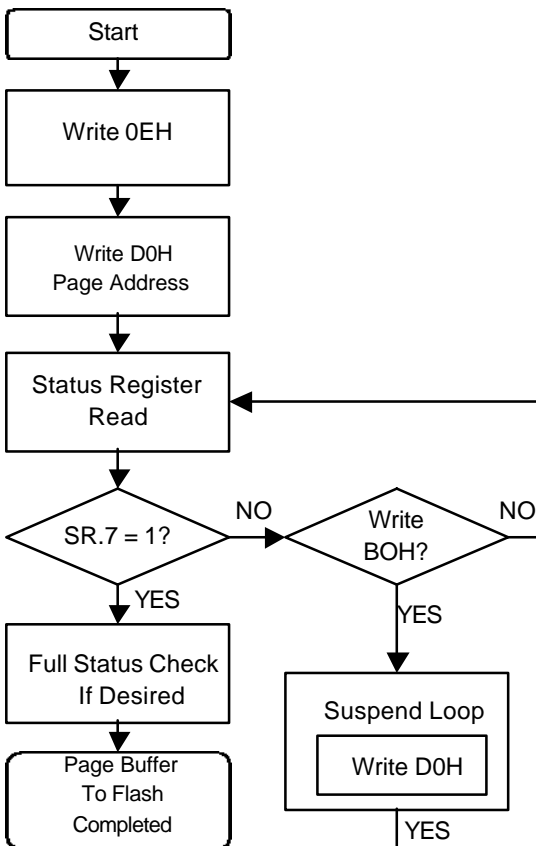
### Single Data Load to Page Buffer Flow Chart



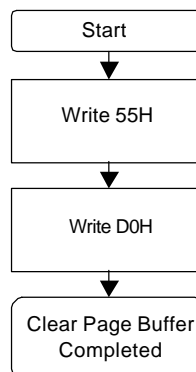
### Suspend / Resume Flow Chart



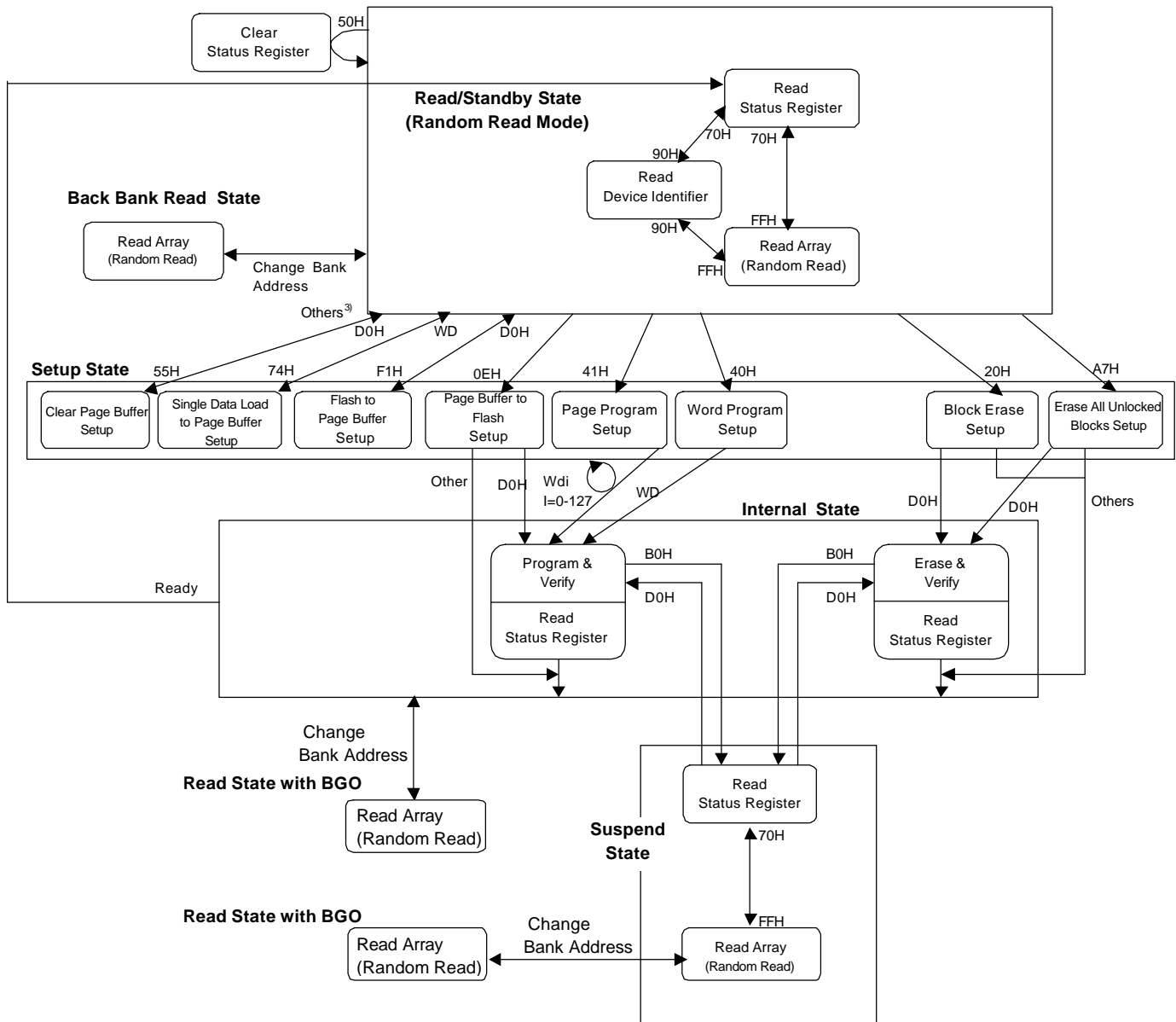
### Page Buffer to Flash Flow Chart



### Clear Page Buffer Flow Chart

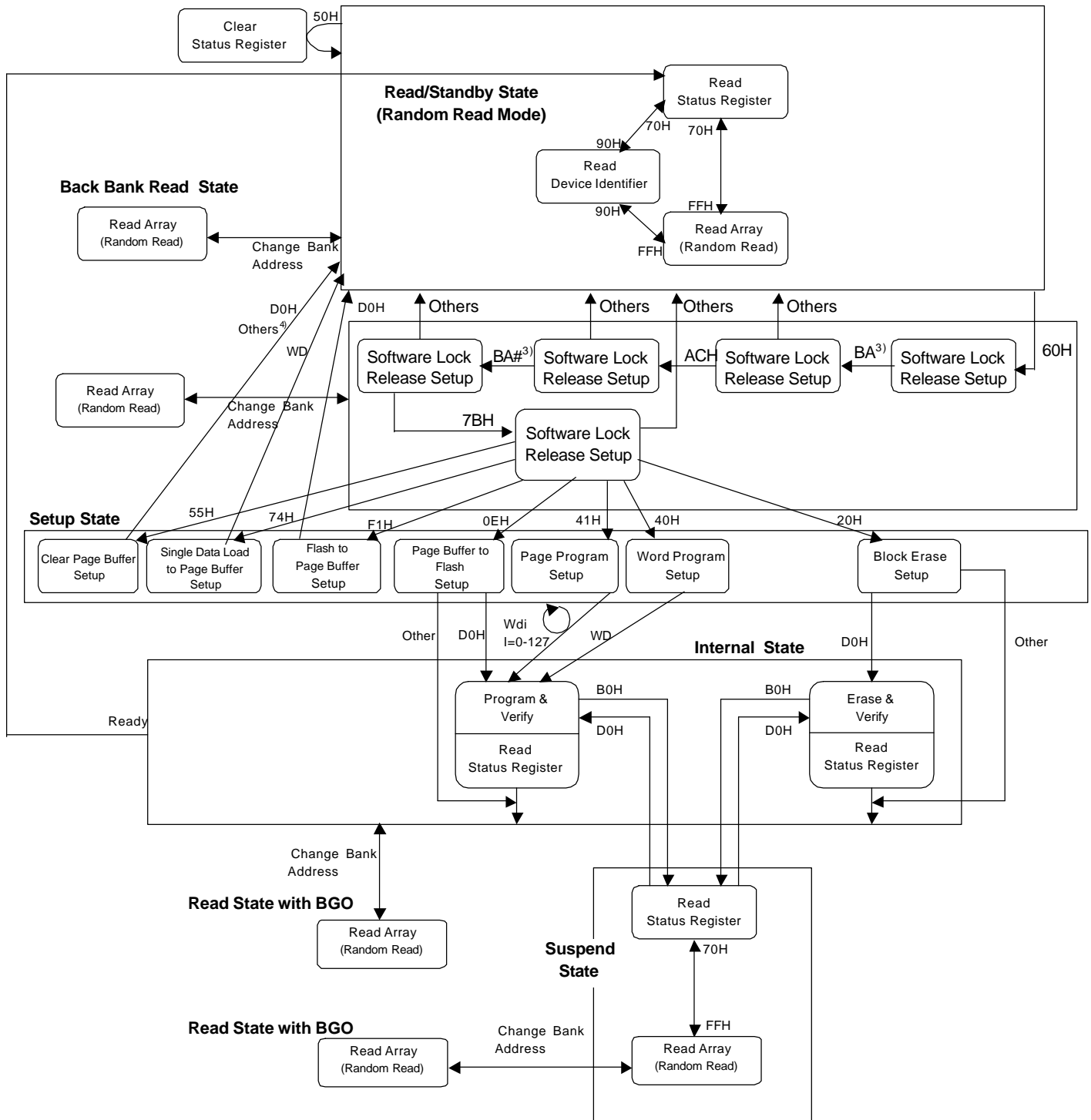


### Operation Status (WP#=VIH)



- 1) In case of Page Read, F3H is used instead of FFH in Operation Status (WP#=VIH).
- 2) Once Page Read mode is set, Page Read mode is kept until power off or RP# is set to VIL.
- 3) After setting up Clear Page Buffer, D0H enables to clear Page Buffer.
- 4) To access any bank during Erase All Unlocked Block results Status Register Read.  
Although Read Status Register Command and Read Array Command can be issued under Suspend State, output data make no sense.

## Operation Status (WP#=VIL)



- 1) In case of Page Read, F3H is used instead of FFH in Operation Status (WP#=VIL).
- 2) Once Page Read mode is set, Page Read mode is kept until power off or RP# is set to VIL.
- 3) BA, BA#: Block Address, Block Address# (Shown in Command List(WP#=VIL) in detail).
- 4) After setting up Clear Page Buffer, D0H enables to clear Page Buffer.

# Preliminary

Notice: This is not a final specification.  
Some parametric limits are subject to change.

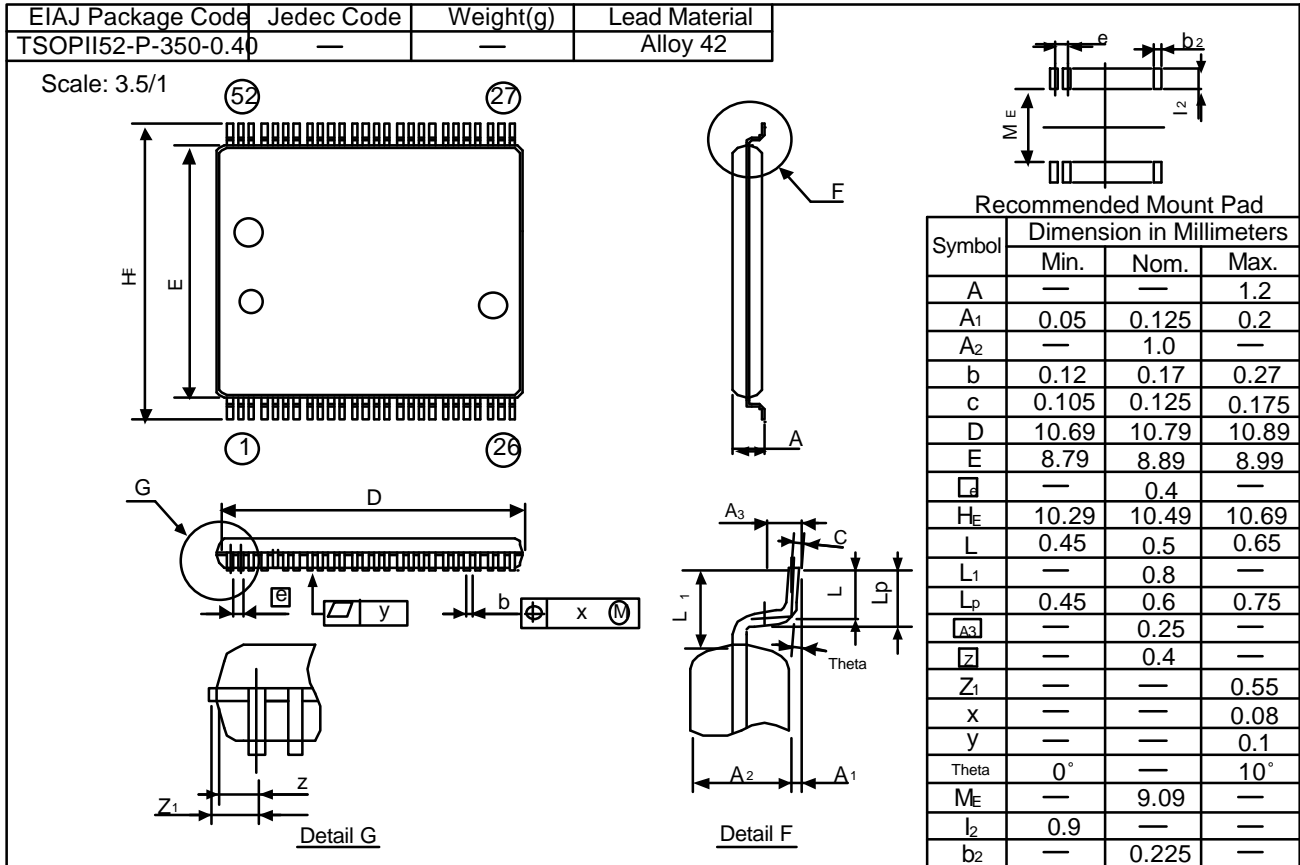
Renesas LSIs

## M5M29KB/T641ATP

67,108,864-BIT (8,388,608-WORD BY 8-BIT /4,194,304-WORD BY 16-BIT)  
CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY

### Package Dimension

52PTG-A





# Preliminary

Notice: This is not a final specification.  
Some parametric limits are subject to change.

Renesas LSIs

## M5M29KB/T641ATP

67,108,864-BIT (8,388,608-WORD BY 8-BIT /4,194,304-WORD BY 16-BIT)  
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## Renesas Technology Corp.

Nippon Bldg.,6-2,Otemachi 2-chome,Chiyoda-ku,Tokyo,100-0004 Japan

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